VIJAYAM INSTITUTE OF TECHNOLOGY

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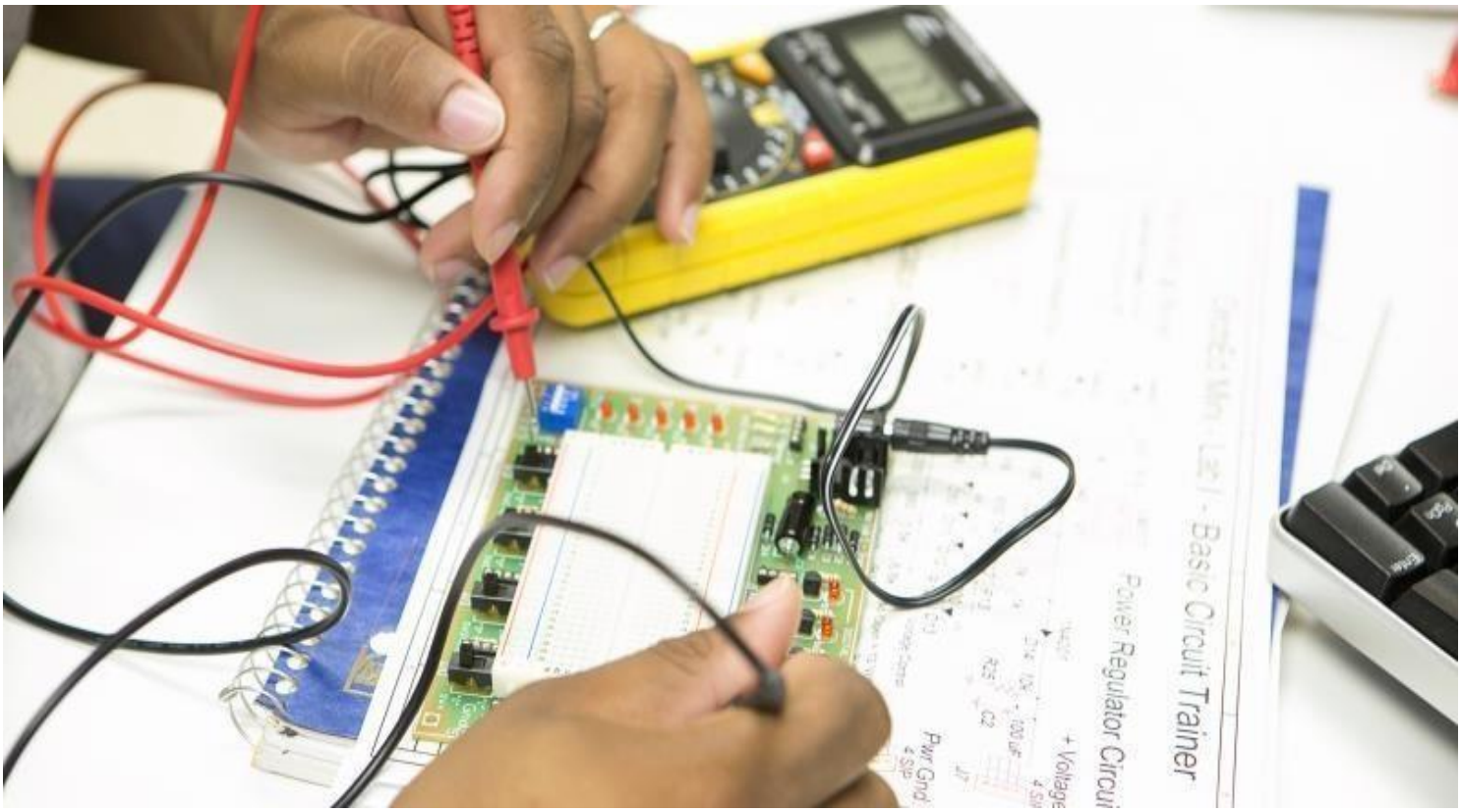
ELECTRICAL AND ELECTRONICS ENGINEERING WORKSHOP

I B.TECH - I Semester **PART-A** **Regulation-R23**



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EXPERIMENT No.: **DATE:**

VERIFICATION OF OHM'S LAW, KIRCHOFF'S VOLTAGE & CURRENT LAW (KVL & KCL)

AIM: To verify the Ohm's law, Kirchoff's voltage law and Kirchoff's current law for a given circuit.

APPARATUS REQUIRED:

SNO.	EQUIPMENT	RANGE	QUANTITY
1.	RPS		
2.	RESISTORS		
3.	AMMETER		
4.	VOLTMETER		
5.	BREAD BOARD		
6	CONNECTING WIRES		

THEORY:-

OHM'S LAW :

The ratio of potential difference (V) between the ends of a conductor to the current (I) flowing between them is constant, provided the physical conditions (e.g. temperature etc.) do not change i.e.

$V / I = \text{Constant} = R\ \Omega$

where *R* is the resistance of the conductor between the two points considered.

KIRCHOFF'S VOLTAGE LAW:

This law relates to e.m.fs and voltage drops in a closed circuit or loop and may be stated as :

In any closed electrical circuit or mesh, the algebraic sum of all the electromotive forces (e.m.fs) and voltage drops in resistors is equal to zero.

In any closed circuit or mesh,

Algebraic sum of e.m.fs + Algebraic sum of voltage drops = 0

KIRCHOFF'S CURRENT LAW:

This law relates to the currents at the *junctions of an electric circuit and stated as :

The algebraic sum of the currents meeting at a junction in an electrical circuit is zero.

PROCEDURE:

OHM'S LAW

1. Connect the circuit as per network shown.
2. Switch on the power supply after giving all the connections.
3. Note down voltmeter and ammeter reading.
4. Calculate the resistance using R = V / I.

KVL

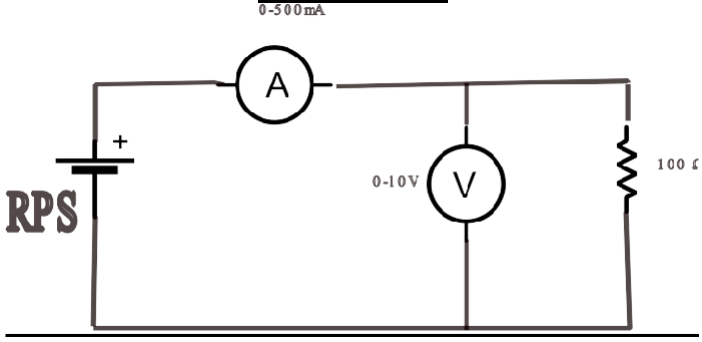
1. Connect the circuit as per network shown.
2. Switch on the power supply after giving all the connections.
3. Adjust the regulated power supply to the rated voltage as mentioned in the circuit.
4. Note down the voltmeter readings.
5. Compare the values of V_1, V_2, V_3 theoretically and practically.

KCL

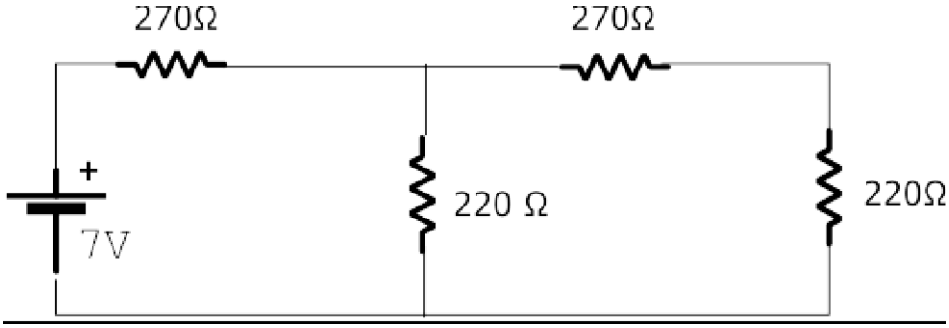
1. Connect the circuit as per network shown.
2. Switch on the power supply and adjust the regulated power supply to the rated voltage as mentioned in the circuit diagram.
3. Note down the ammeter readings.
4. Compare the values of I_1, I_2, I_3 theoretically and practically.

CIRCUIT DIAGRAM:

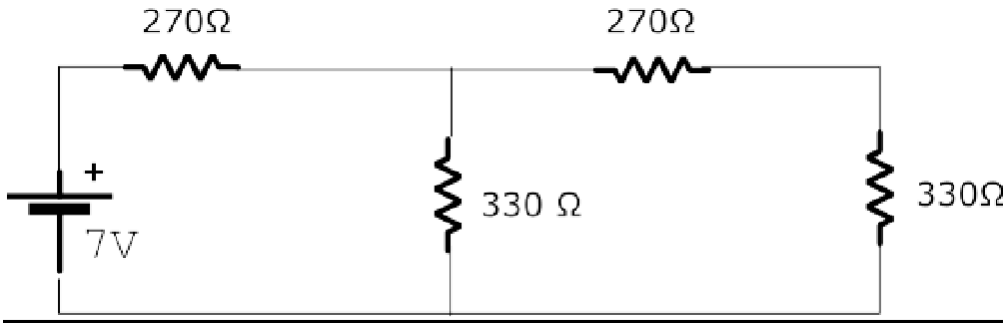
OHM'S LAW



KVL

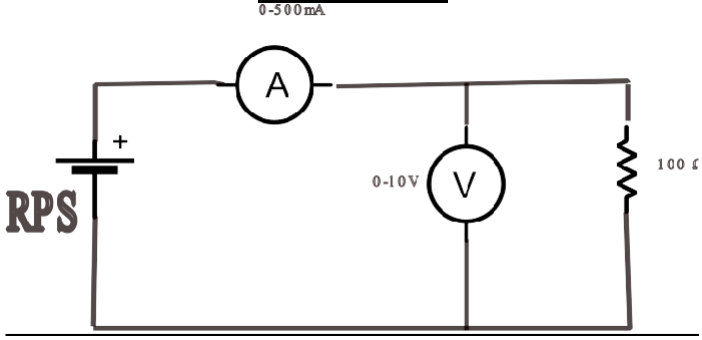


KCL

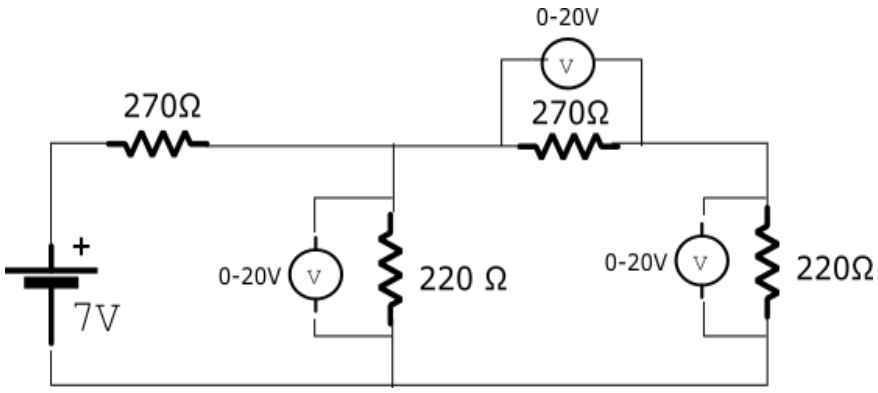


CONNECTION DIAGRAM:

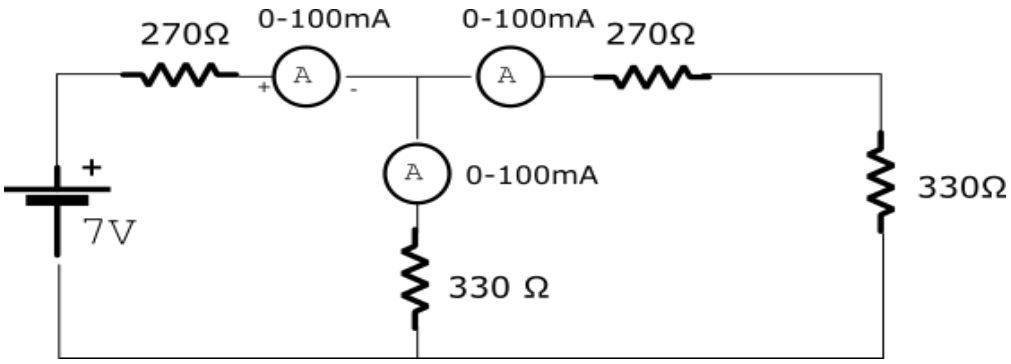
OHM'S LAW



KVL



KCL



TABULAR COLUMN:
FOR OHM'S LAW

Sl No.	V (volts)	I (Amp)	R= V / I (Ω)
		Average R	

FOR KVL

	V_1(volts)	V_2(volts)	V_3(volts)	V(volts)
THEORETICAL				
PRACTICAL				

FOR KCL

S.No.	I_1(mA)	I_2(mA)	I_3(mA)	I(mA)
THEORETICAL				
PRACTICAL				

RESULT:

EXPERIMENT No: **DATE:**

VERIFICATION OF SUPERPOSITION THEOREM

AIM: To verify Superposition theorem for a given circuit.

APPARATUS REQUIRED:

SNO.	EQUIPMENT	RANGE	QUANTITY
1.	RESISTORS		
2.	AMMETER		
3.	R.P.S		
4.	BREAD BOARD		
5.	CONNECTING WIRES		

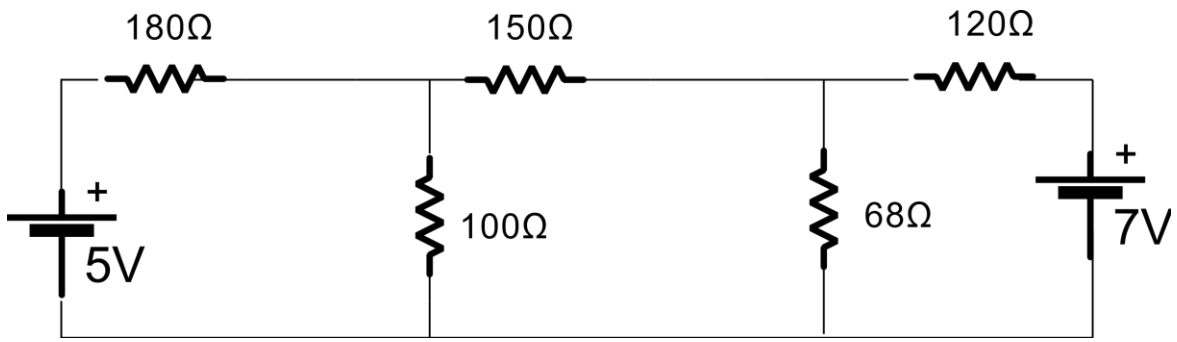
PROCEDURE:

SUPERPOSITION THEOREM

1. Connections are made as per the circuit diagram.
2. By replacing current source by open circuit i.e. replace current source by internal resistance the ammeter readings I'_1 and I'_2 is measured.
3. By replacing voltage source by short circuit i.e. replace voltage source by internal resistance the ammeter readings I''_1 and I''_2 is measured.
4. Measure currents I_1 and I_2 with both sources connected.
5. Theoretical values are compared with the measured values.

CIRCUIT DIAGRAM

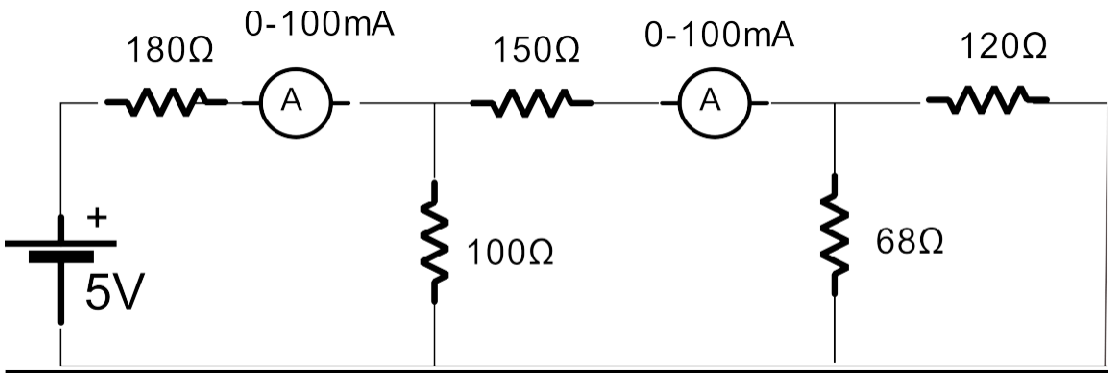
SUPERPOSITION THEOREM



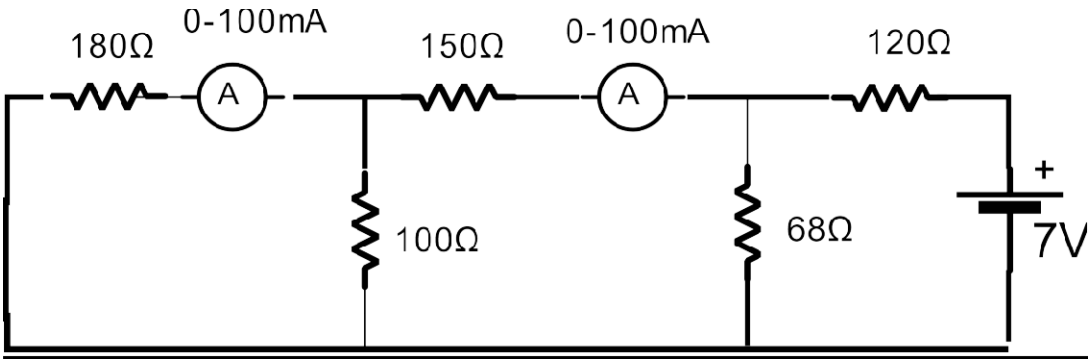
CONNECTION DIAGRAMS:

SUPERPOSITION THEOREM

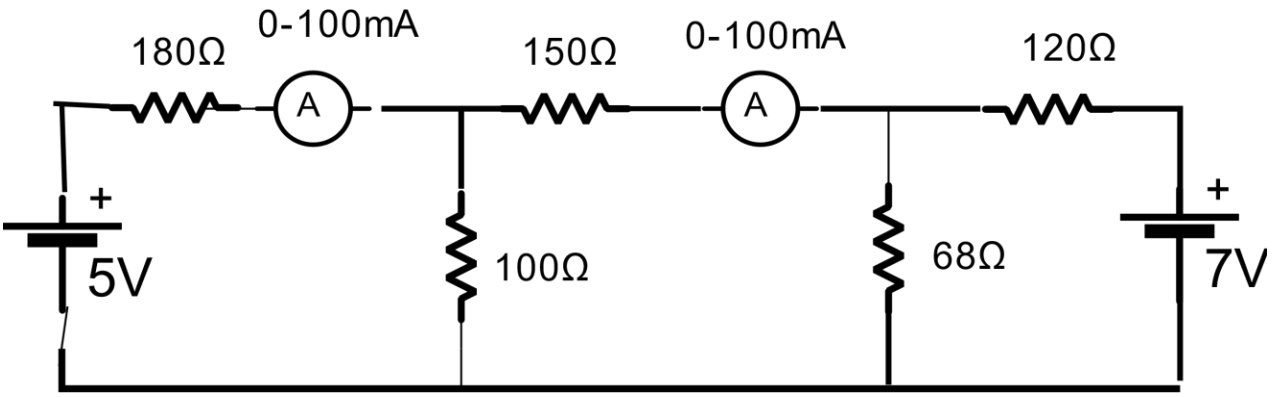
VOLTAGE SOURCE V_1 ACTING ALONE:



VOLTAGE SOURCE V_2 ACTING ALONE:



BOTH SOUIRCES ACTING



TABULAR COLUMN:

SUPERPOSITION THEOREM

		THEORETICAL	PRACTICAL
VOLTAGE SOURCE V_1 ACTING	I_1'		
	I_2'		
VOLTAGE SOURCE V_2 ACTING	I_1''		
	I_2''		
BOTH SOURCES	$I_1 = (I_1' + I_1'')$		
	$I_2 = (I_2' + I_2'')$		

RESULT :

EXPERIMENT NO: **DATE:**

MEASUREMENT OF RESISTANCE USING WHEATSTONE BRIDGE

AIM: To find unknown resistance value using Wheatstone bridge.

APPARATUS REQUIRED:

Sl No.	Item	Quantity
1	Wheatstone bridge	
2	Decade Resistance Box or Resistances	
3	Multimeter	
4	Patch cords	

Formula:

$$R_x = \frac{R_1}{R_2} \times R_3$$

PROCEDURE:

1. Connections are made as per connection diagram
2. Connect the Decade Resistance Box or Resistance at R_x terminal
3. Switch-on the bridge and vary resistance at R_1 and R_3 to get the nearest point of balance.
4. Now vary R_2 to get exact point of balance.
5. Switch-off the bridge and remove patch chord at R_2 .
6. Now measure the resistance R_2 using multimeter.
7. Tabulate the readings and find the value of unknown resistance.

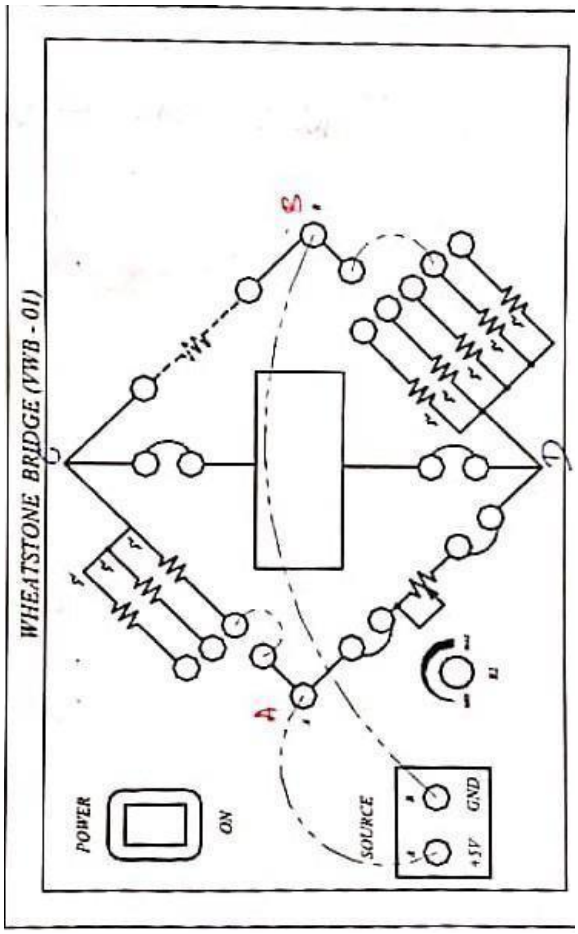
TABLE

S. No	R_1 Ω	R_2 Ω	R_3 Ω	R_x Ω (Practical)	R_x Ω (Theoretical)

RESULT:

Thus the value of unknown resistance was measured using Wheatstone bridge.

CIRCUIT DIAGRAM:



EXP.NO: **DATE:**

MAGNETIZATION CHARACTERISTICS OF DC SHUNT GENERATOR

1. AIM: To draw the open circuit characteristic of the given DC shunt generator at its rated speed and to determine the critical resistance and critical speed.

2. NAME PLATE DETAILS:

3. APPARATUS REQUIRED:

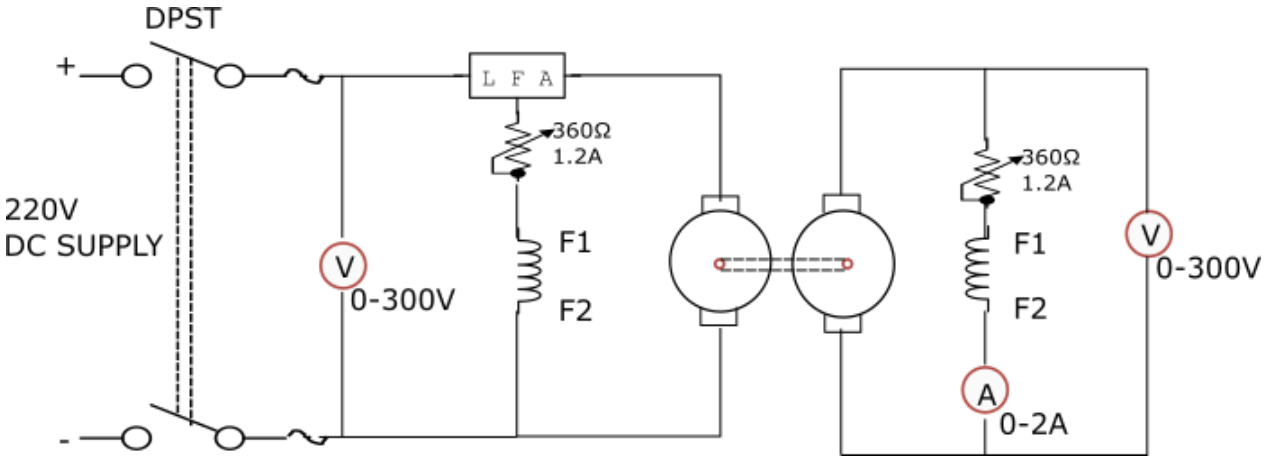
PRECAUTIONS:-

1. The starter should be in OFF position before switching on the supply
2. Field rheostat of the motor should be kept at minimum resistance position
3. Field rheostat of the generator should be kept at maximum resistance positon

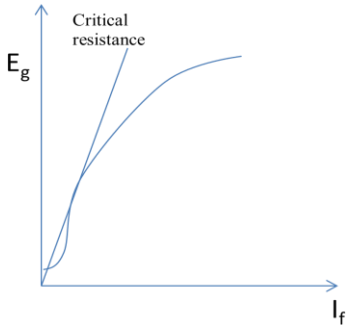
PROCEDURE:-

1. Make connections as shown in the circuit diagram.
2. Observe all precautions and switch on the supply.
3. Start the motor using starter and note the speed.
4. Adjust the field rheostat of the motor and bring the speed of the generator to its rated speed.
5. Note whether there is any residual voltage indicated by the voltmeter.
6. Reduce the resistance of the generator field rheostat gradually noting whether armature terminal voltage increasing.
7. If the residual voltage is decreasing, reverse the generator field terminals.
8. Adjust the generator field rheostat for various increasing values of field current in steps of 0.05A up to maximum armature voltage.

CIRCUIT DIAGRAM



Model GRAPH



TABULAR COLUMN & GRAPHS:

Sl.No.	Field Current (I_f) Amps	Generated voltage Volts

RESULT:

EXPERIMENT NO: **DATE:**

MEASUREMENT OF POWER AND POWER FACTOR USING A SINGLE PHASE WATTMETER

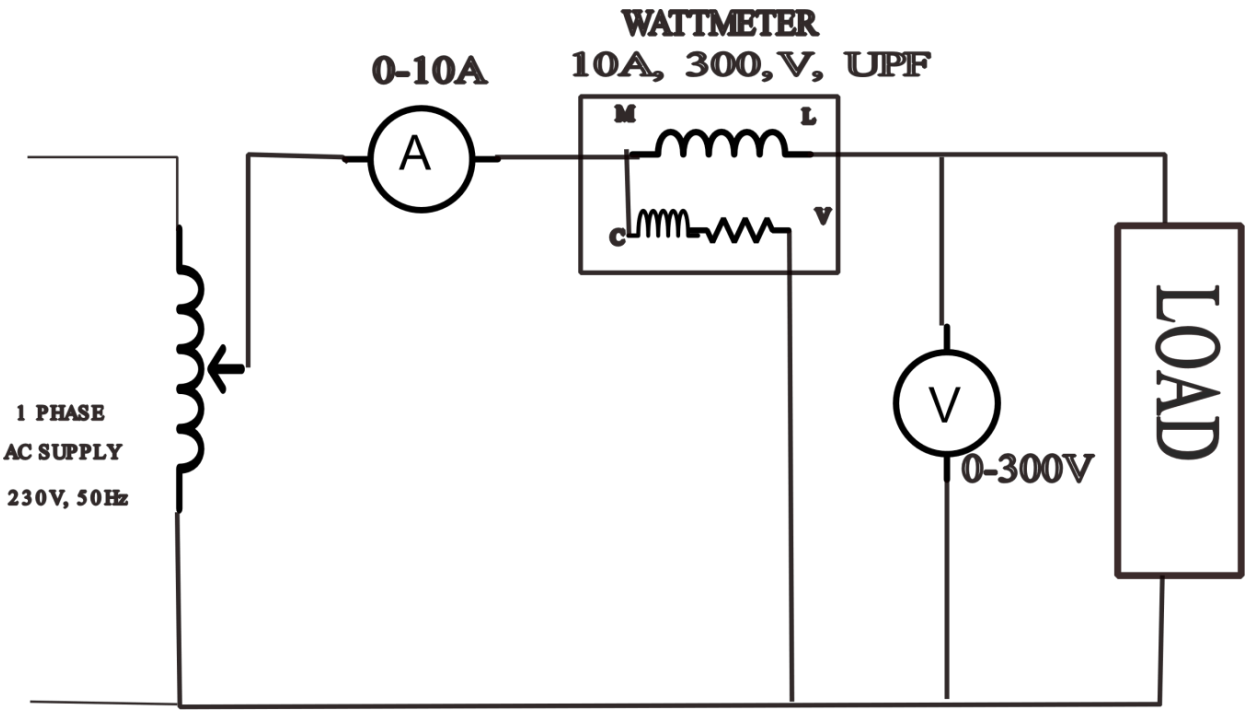
AIM:

Measurement of power and power factor in a single phase ac using wattmeter.

APPARATUS REQUIRED:

Sl. No.	Name	Specification	Quantity
1	Single-phase auto transformer	5KVA, (0-270)V	1 Nos.
2	Voltmeter	(0-300)V, MI	1 Nos.
3	Watt-meter	(0-1500)W,	1 Nos.
4	Ammeter	(0-10)A, MI	1 Nos.
5	Resistive load	1kW	1 Nos.
6	Capacitive load		1 Nos.
7	Inductive load		
8	Connecting Wires	-	As per required

CIRCUIT DIAGRAM:



THEORY:

Power consumed by the load is given by

$$P = VI\ cos\varphi$$

$$Power\ factor = cos\varphi = \frac{P}{VI}$$

where,

P - active power in watt,

V - supplied voltage in volts,

I - current flowing through the circuit elements in Amp.

Using above formula the power consumed by the load and power factor can be determined.

PROCEDURE:

1. Connect all the instruments as per circuit diagram given above.
2. Before switch on the main power supply make sure that single-phase auto transformer is at zero position.
3. Now change the load value by varying resistance bank.
4. Take all the corresponding readings of the connected instruments in the circuit as per observation table.
5. Now calculate power factor (cosϕ) as per formula given in observation table.

TABULAR COLUMN:

Sl. No.	V (in volts.)	I (in Amp.)	P (in watts.)	cosϕ= {P/(V*I)}
1				
2				
3				
4				
5				

RESULT:

EXPERIMENT NO: **DATE:**

MEASUREMENT OF EARTH RESISTANCE USING MEGGER

AIM: To measure the earth resistance using megger.

APPARATUS REQUIRED:

SL NO	NAME OF EQUIPMENT	RANGE	QUANTITY
1	Megger	-	1
2	Spikes	-	2
3	Connecting wires	-	--

THEORY:

All the electrical installations and appliances should be earthed properly for ensuring human safety. A separate wire, known as earth wire runs along the supply line and is connected to the ground through an earth electrode. The total resistance of the earthing system should be small so that in the event of any fault, the fault current is sufficiently high to blow off the fuse. The earth resistance is the resistance offered by the soil and the electrode to the flow of earth leakage current, which will flow in case of earth fault only.

The earth tester is a special type of ohmmeter which sends ac through earth and dc through the measuring instruments as shown in Fig. The direction of flow of current in the ground keeps on alternating due to current reverse whereas current directions in the two reverser and potential reverser are mounted on the main shaft of hand driven dc generator.

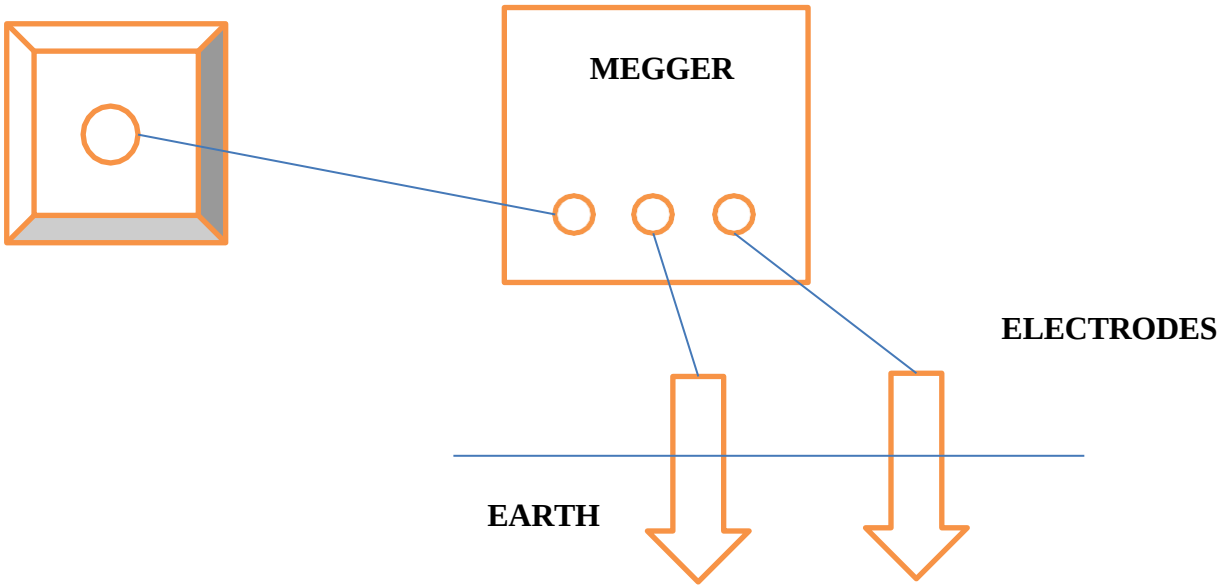
The working principle of an earth tester is identical to that of megger. There are two moving coil viz. potential and current coil, which are deflected in the magnetic field of a permanent magnet. The hand driven generator or a set of batteries supply power to these coils. It has three terminals E , U , a nd H . Terminal E is connected to the earth electrode under test. The other two terminals U and H are connected to the auxiliary electrode A and B respectively. At the side of the megger two press buttons show 3Ω, 30Ω select any suitable one. The value of earth resistance is indicated directly on the scale when the generator arm is rotated.

The value of earth resistance depends upon the soil condition and its moisture contents. In hilly areas the earth resistance is higher if electrodes are not place properly in contact with the

earth. Water content in the soil decreased the earth resistance. The normal value of earth resistance should lie between 1 to 2Ω.

CIRCUIT DIAGRAM:

EARTH PIT TO BE TESTESD



PROCEDURE:

1. Connect the megger as shown in diagram
2. Switch ON the megger.
3. Adjust the resistance range button 3Ω or 30Ω .
4. Change the position of electrodes U and H by 1m on the either side and observe the earth resistance.
5. Draw the graph and find Earth Resistance.

TABULAR COLUMN

S.No	Distance	Resistance

RESULT:

Thus the earth resistance is measured using megger and plotted the graph.

EXPERIMENT NO: **DATE:**

CALCULATION OF ELECTRICAL ENERGY FOR DOMESTIC PREMISES

AIM: To study the construction and working of single phase energy meter and to find out energy consumed.

APPARATUS REQUIRED:

SL NO	NAME OF EQUIPMENT	RANGE	QUANTITY
1	Single phase energy meter	-	1
2	Light load	-	1
3	Singlephase Induction motor		1
4	Fan		
5	Connecting wires	-	--

Working Principle

Energy meter is an instrument which measures electrical energy. It is also known as watt-hour (Wh) meter. It is an integrating device. There are several types of energy meters single phase induction type energy meter are very commonly used to measure electrical energy consumed in domestic and commercial installation. Electrical energy is measured in kilo watt-hours (kWh) by this energy meter.

Construction: A single phase induction type energy meter consists of driving system, moving system, braking system and registering system. Each of the systems is briefly explained below.

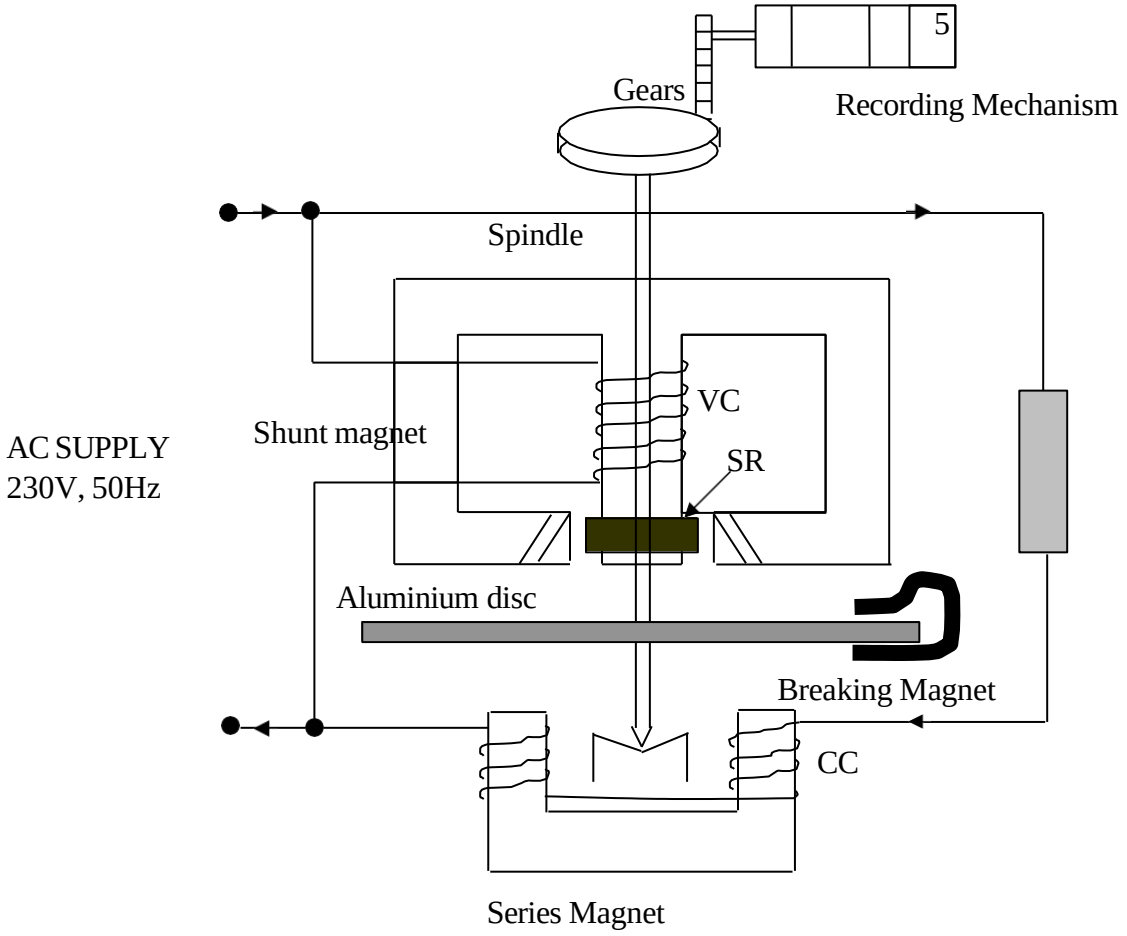
Driving system: This system of the energy meter consists of two silicon steel laminated electromagnets. M1 & M2 as shown in fig.1The electromagnet M1 is called the series magnet and the electromagnet M2 is called the shunt magnet. The series magnet M1 carries a coil consisting of a few turns of thick wire. This coil is called the current coil (CC) and it is connected in series with the circuit. The load current flows through this coil. The shunt magnet M2 carries a coil consisting many turns of thin wire. This coil is called the voltage coil (VC) and is connected across the supply it consist of current proportional to the supply voltage. Short circuited copper bands are provided on the lower part of the central limb of the shunt magnet. By adjusting the position of these loops the shunt magnet flux can be made to lag behind the supply voltage exactly 90 . These copper bands are called power factor compensator (PFC). A copper shading band is provided on each outer limb of the shunt magnet (fc1 &fc2) these band provides frictional compensation.

Moving system: The moving system consists of a thin aluminum disc mounted on a spindle and is placed in the air gap between the series and the shunt magnets. It cuts the flux of both the magnet forces are produced by the fluxes of each of the magnets with the eddy current

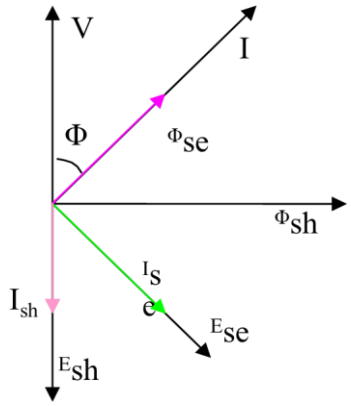
induced in the disc by the flux of the other magnets. Both these forces act on the disc. These two forces constitute a deflecting torque.

Braking system: - The braking system consists of a permanent magnet called brake magnet. It is placed near the edge of the disc as the disc rotates in the field of brake magnet eddy current are induced in it. These eddies current react with the flux and exert a torque. This torque acts in direction so that it opposes the motion of disc. The braking torque is proportional to the speed of the disc.

Registering system: - the disc spindle is connected to a counting mechanism this mechanism records a number which is proportional to the number of revolutions of the disc the counter is calibrated to indicate the energy consumed directly in kilo watts-hour (kWh)



VC – Voltage coil
CC – Current coil
SR – Shading ring



V=Supply voltage

I=Load current lagging behind V by Φ

Cos Φ = Load Power Factor (Lagging)

I_{sh}= Current setup by Φ_{sh} in disc

I_{se}= Current setup by Φ_{se} in disc

$\tau_d \propto (\psi_{sh} i_{se} - \psi_{se} i_{sh})$ where ψ & i are instantaneous values

Average deflecting toque

$T_d \propto [\Phi_{sh} I_{se} \cos\Phi - \Phi_{se} I_{sh} \cos(180-\varphi)]$ where Φ & I are RMS values

$T_d \propto [\Phi_{sh} I_{se} \cos\Phi + \Phi_{se} I_{sh} \cos\varphi]$

$T_d \propto [\Phi_{sh} I_{se} + \Phi_{se} I_{sh}] \cos\varphi$

We know

$\Phi_{sh} \propto V$, $I_{se} \propto I$, $\Phi_{se} \propto I$, $I_{sh} \propto V$ So

Average deflection torque

$T_d \propto VI \cos\varphi$

$\propto$ Power

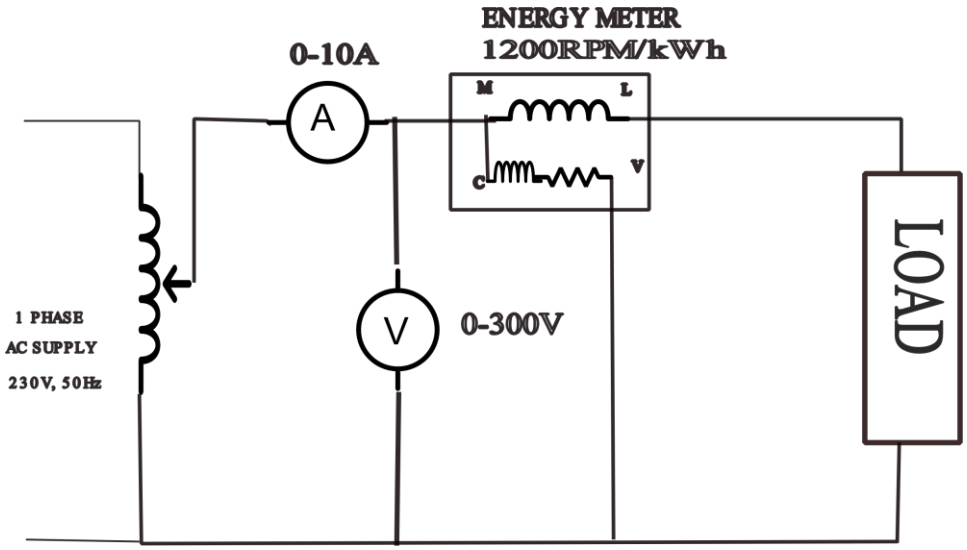
No of revolution made in t sec

$$\int_0^t Ndt = \int_0^t Pdt \text{ a } Energy\ consumed\ in\ t\ sec$$

Meter Constant

$$K = \frac{Revolutions\ made}{kWh}$$

CIRCUIT DIAGRAM:



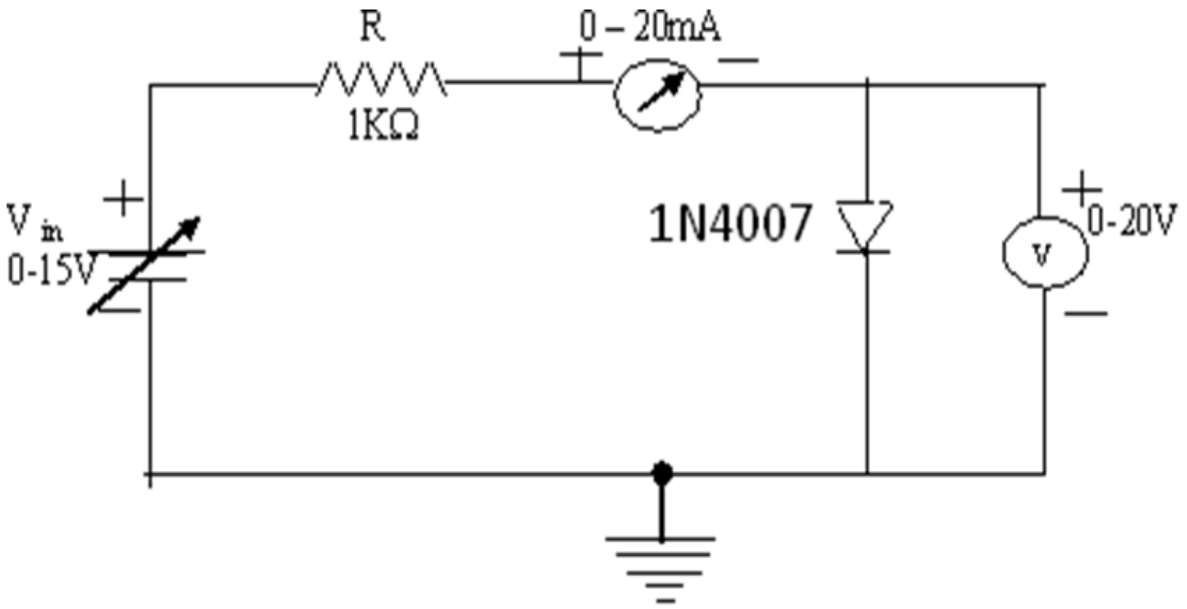
TABULAR COLUMN:

S.No.	Time for one revolution (sec)	V_L (Volts)	I_L (Amps)	Type of load	kWh

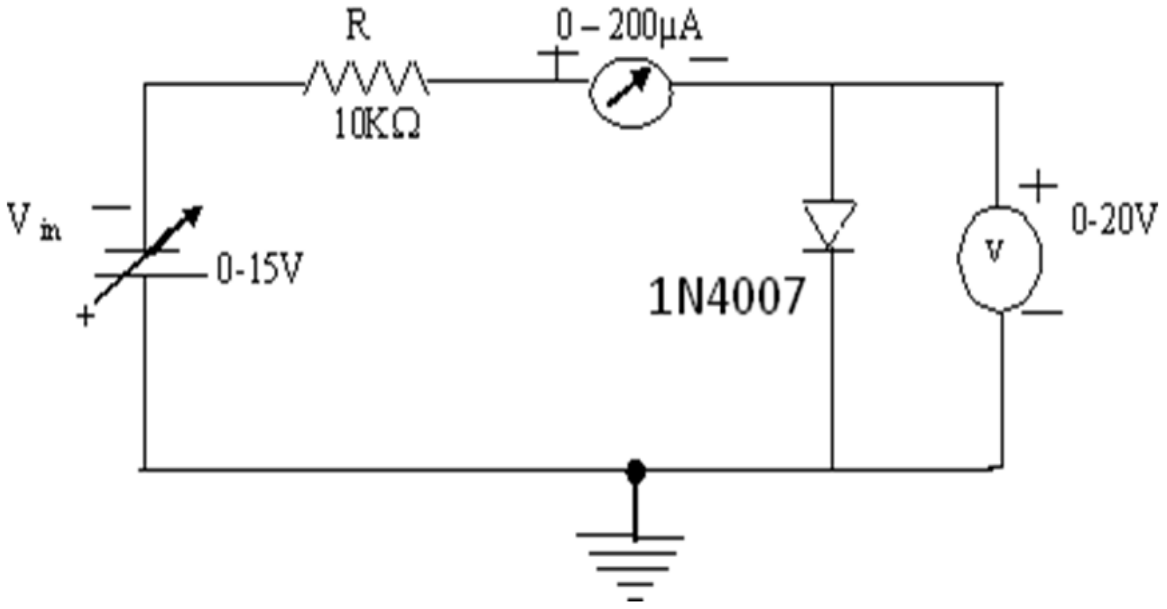
$$kWh = \frac{No\ of\ revultions}{1200} \times \frac{Time\ (secs)}{60 \times 60}$$

PART – B

Forward baised :-



Reverse baised :-



EXPERIMENT NO: *DATE:*

PLOT V-I CHARACTERISTICS OF PN JUNCTION DIODE

AIM:- To observe and draw the Forward and Reverse bias V-I Characteristics of a PN Junction diode.

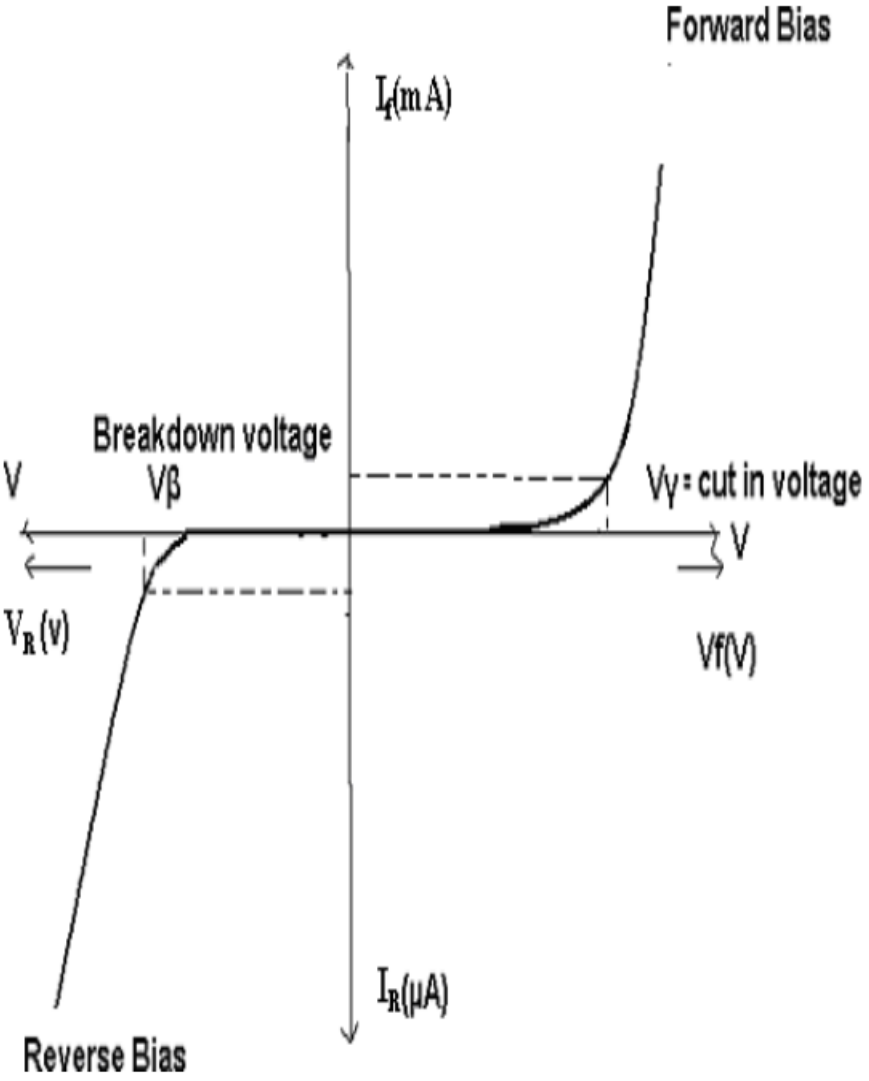
COMPONENTS & EQUIPMENT REQUIRED :

S.NO	NAME OF THE EQUIPMENT	RANGE	QUANTITY
1	PN junction Diode	1N 4007	1
2	Resistor	1KΩ	1
3	Regulated Power supply	(0-30)V	1
4	Ammeters	(0-20) mA, (0-500)µA	1
5	Volt meter	(0-2)V,(0-20)V	1
6	Connecting wires	-	As per required
7	Bread board	-	1

THEORY:-

A p-n junction diode conducts only in one direction. The V-I characteristics of the diode are curve between voltage across the diode and current through the diode. When external voltage is zero, circuit is open and the potential barrier does not allow the current to flow. Therefore, the circuit current is zero. When P-type (Anode is connected to +ve terminal and n- type (cathode) is connected to –ve terminal of the supply voltage, is known as forward bias. The potential barrier is reduced when diode is in the forward biased condition. At some forward voltage, the potential barrier altogether eliminated and current starts flowing through the diode and also in the circuit.
The diode is said to be in ON state. The current increases with increasing forward voltage.
When N-type (cathode) is connected to +ve terminal and P-type (Anode) is connected –ve terminal of the supply voltage is known as reverse bias and the potential barrier across the junction increases. Therefore, the junction resistance becomes very high and a very small current (reverse saturation current) flows in the circuit. The diode is said to be in OFF state. The reverse bias current due to minority charge carriers.

Model Waveform :-



PROCEDURE:-

FORWARD BIAS:-

1. **Connections are made as per the circuit diagram.**
2. **For forward bias, the RPS +ve is connected to the anode of the diode and RPS –ve is connected to the cathode of the diode,**
3. **Switch on the power supply and increase the input voltage (supply voltage) in Steps.**
4. **Note down the corresponding current flowing through the diode and voltage across the diode for each and every step of the input voltage.**
5. **The reading of voltage and current are tabulated.**
6. **Graph is plotted between voltage and current.**

REVERSE BIAS:-

1. Connections are made as per the circuit diagram

2 .For reverse bias, the RPS +ve is connected to the cathode of the diode and RPS –ve is connected to the anode of the diode.

3. **Switch on the power supply and increase the input voltage (supply voltage) in Steps**
4. **Note down the corresponding current flowing through the diode voltage across the diode for each and every step of the input voltage.**
5. **The readings of voltage and current are tabulated**

Graph is plotted between voltage and current.

TABULAR COLUMN:-

FORWARD BIAS:

S. No	VF (Volts)	IF (m A)
1		
2		
3		
4		
5		
6		
7		
8		
9		
10		
11		
12		
13		

REVERSE BIAS:

S. No.	VR (Volts)	IR (µ A)
1		
2		
3		
4		
5		
6		
7		
8		
9		
10		
11		
12		
13		

PRECAUTIONS:-

1. All the connections should be correct.
2. Parallax error should be avoided while taking the readings from the Analog meters.

CALCULATIONS:-

1. Static Forward Resistance R F = (V/ I) Ω.

2.Dynamic Forward Resistance r f = $\Delta V / \Delta I$ Ω.

3. Static Reverse Resistance R r = (V/ I) Ω.

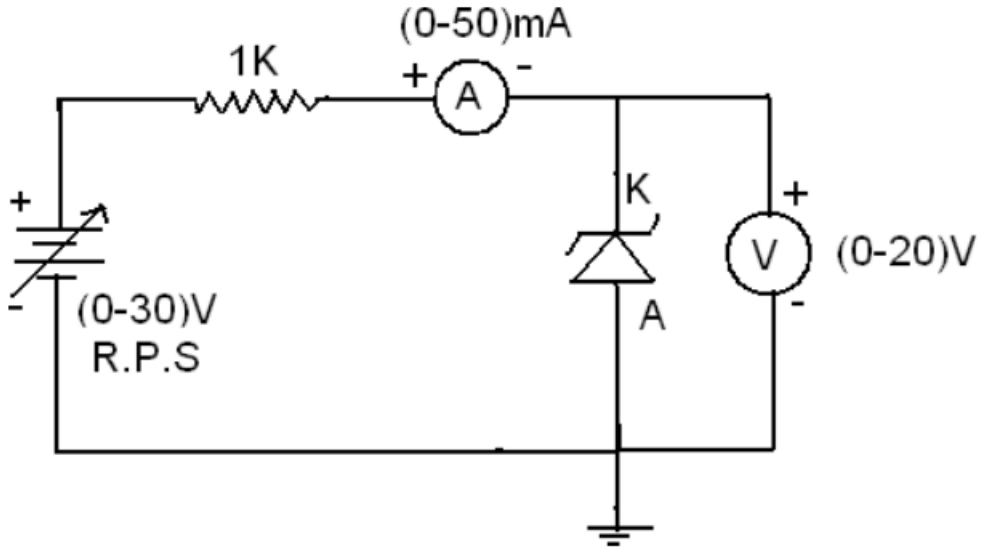
4. Dynamic Reverse Resistance R r = $\Delta V / \Delta I$ Ω.

RESULT:-

Forward and reverse bias characteristics for PN diode was observed

1. Static Forward Resistance R_{Fr}=
2. Dynamic Forward Resistance D_{Fr} =
3. Static Reverse Resistance R_{r} =
4. Dynamic Reverse Resistance D_{Rr} =

Circuit Diagram :-



EXPERIMENT NO: ***DATE:***

ZENER DIODE CHARACTERISTICS AS A VOLTAGE REGULATOR

AIM:- a) To observe and draw the static characteristics of a Zener diode

b) To verify Zener diode as the voltage regulator

COMPONENTS & EQUIPMENT REQUIRED *:*

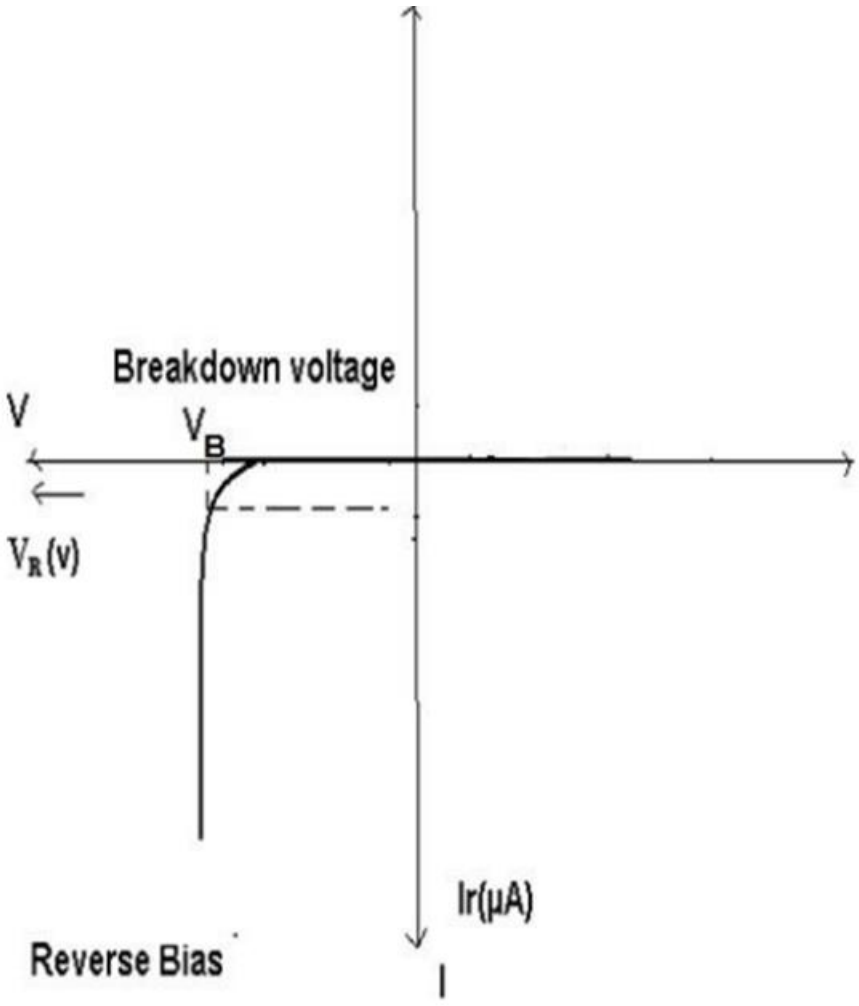
S.NO	NAME OF THE EQUIPMENT	RANGE	QUANTITY
1	Zener diode.	BZVC 6.2	1
2	Regulated Power Supply	(0-30)V	1
3	Voltmeter	(0-20)V	1
4	Ammeter	(0-50) mA	1
5	Resistor	1KΩ	1
6	Bread board	-	1
7	Connecting Wires	-	Few

THEORY:-

A zener diode is heavily doped p-n junction diode, specially made to operate in the break down region. A p-n junction diode normally does not conduct when reverse biased. But if the reverse bias is increased, at a particular voltage it starts conducting heavily. This voltage is called Break down Voltage. High current through the diode can permanently damage the device.

To avoid high current, we connect a resistor in series with zener diode. Once the diode starts conducting it maintains almost constant voltage across the terminals what ever may be the current through it, i.e., it has very low dynamic resistance. It is used in voltage regulato

MODEL WAVEFORMS:-



PROCEDURE:

REVERSE BIAS: -

1. Connect the circuit as per the circuit diagram.
2. Vary the power supply voltage Note down the corresponding
3. Ammeter and Voltmeter readings.
4. Plot the graph between VR and IR.
5. Calculate static resistance of the zener diode

PRECAUTIONS: -

1. The terminals of the zener diode should be properly identified
2. Should be ensured that the applied voltages & currents do not exceed the ratings of the diode.

TABULAR COLUMN:

REVERSE BIAS:

S. No	VR (Volts)	IR(µ A)
1		
2		
3		
4		
5		
6		
7		
8		
9		
10		
11		
12		
13		

CALCULATIONS:-

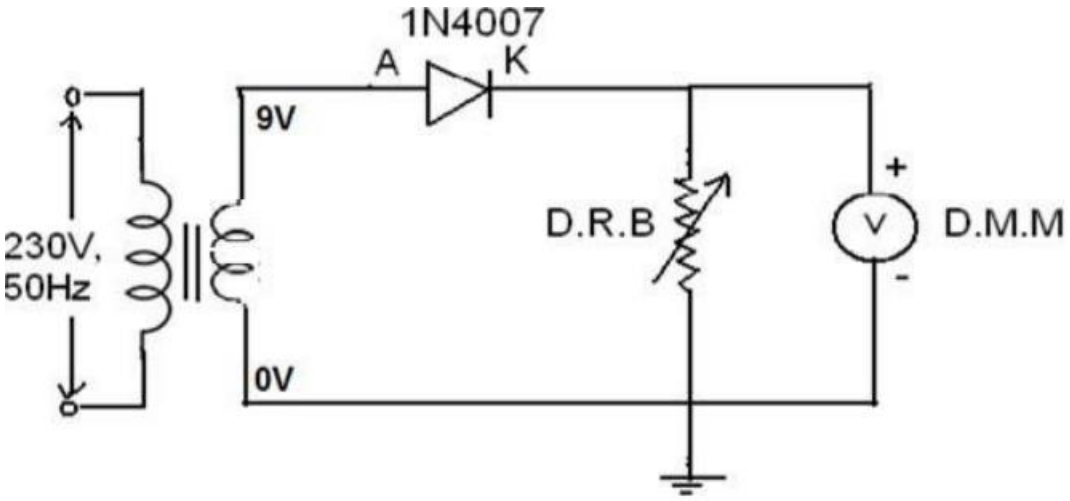
Static Reverse Resistance $R_r = (V/ I) \Omega$. .=

RESULT:- :-

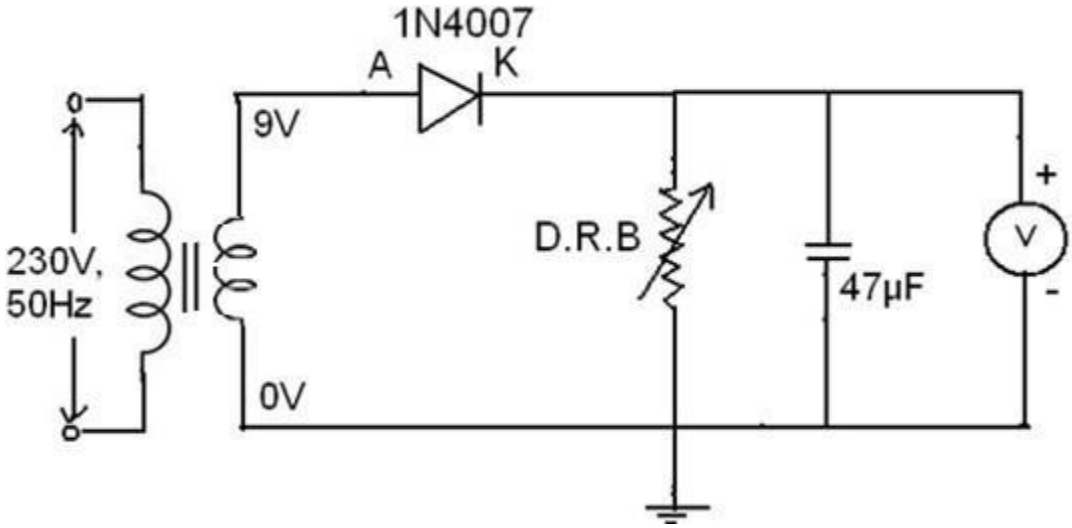
The static characteristics of a zener diode has been observed and drawn.
Static Reverse Resistance R r = Break down voltage =

CIRCUIT DIAGRAM:-

WITHOUT FILTER:-



WITH FILTER:-



EXPERIMENT NO: ***DATE:***

HALF WAVE RECTIFIER WITH OUT AND WITHFILTER

AIM*: -* *T*o obtain the load regulation and ripple factor of a Half-Wave Rectifier.

1. without Filter
2. with Filter

COMPONENTS & EQUIPMENT REQUIRED *:*

S.NO	NAME OF THE EQUIPMENT	RANGE	QUANTITY
1	Transformer	230V/(0-9)V.	1
2	Diode	1N 4007	1
3	Capacitor	47μf	1
4	Resistor	1KΩ.	1
5	Multimeter	-	1
6	Conncting wires	-	As per required

THEORY: -

During positive half-cycle of the input voltage, the diode D1 is in forward bias and conducts through the load resistor R1. Hence the current produces an output voltage across the load resistor R1, which has the same shape as the +ve half cycle of the input voltage.
During the negative half-cycle of the input voltage, the diode is reverse biased and there is no current through the circuit. i.e, the voltage across R1 is zero. The net

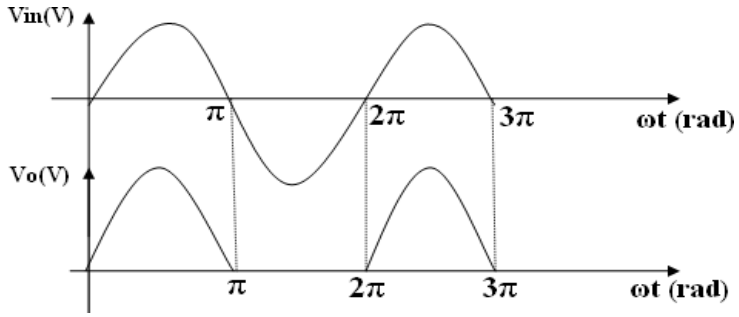
result is that only the +ve half cycle of the input voltage appears across the load. The average value of the half wave rectified o/p voltage is the value measured on dc voltmeter.

For practical circuits, transformer coupling is usually provided for two reasons.

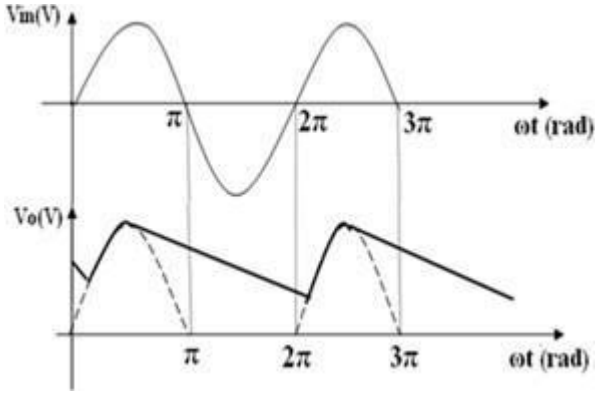
1. The voltage can be stepped-up or stepped-down, as needed.
2. The ac source is electrically isolated from the rectifier. Thus preventing shock hazards in the secondary circuit.

MODEL INPUT & OUTPUT WAVE FORMS:-

WITHOUT FILTER :

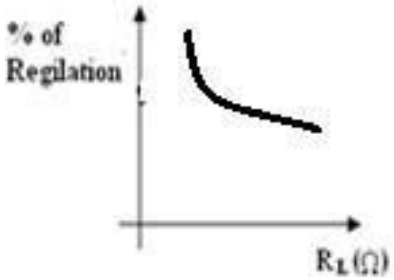


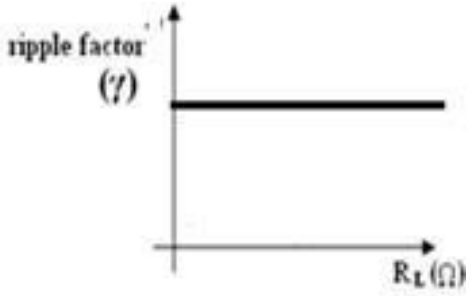
WITH FILTER :



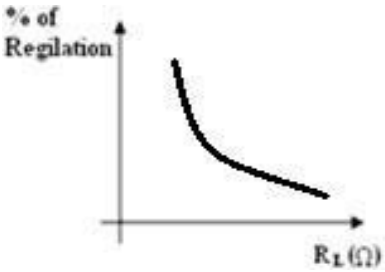
MODEL GRAPHS:

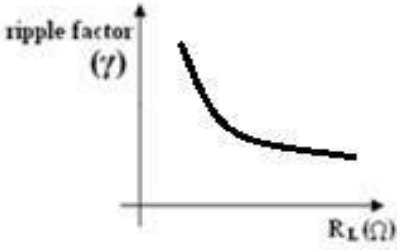
WITHOUT FILTER





WITH FILTER





PROCEDURE:

1. Connect the circuit as per the circuit diagram shown in Figure..
2. Note down the No Load DC Voltage Vdc0 when Idc = 0
3. Vary the load resistance RL (DRB) and note down Idc and Vdc, Vac Using Multimeter

a). Calculate the ripple factor (r)

$$r = \frac{\text{RMS valuesof A Ccomponent} = Vac}{\text{Average value} \quad Vdc}$$

b). Calculate the Percentage of Regulation = [(Vd c 0 – Vdc) / Vdc] x 100 (or) (VNL – VFL) / VFL X 100

4. Draw the following graphs
   i). RL Vs Ripple factor
   ii) RL Vs % regulation.

TABULAR COLUMN:-
WITHOUT FILTER :

No Load voltage= 4.12V

S.No.	RL (W)	Idc (mA)	Vdc (V)	Vac (V)	Ripple Factor r = Vac/Vdc	% of Voltage Regulation = [(Vdco – Vdc)/Vdc] X100
1						
2						
3						
4						
5						
6						
7						
8						
9						

TABULAR COLUMN:-
WITHFILTER :

No Load voltage=11.75V

S.No.	**RL (**W**)**	**Idc (mA)**	**Vdc (V)**	**Vac (V)**	**r = Vac/Vdc**	**% of Regulation = [(Vdco – Vdc)/Vdc] X100**
1						
2						
3						
4						
5						
6						
7						
8						
9						

RESULT:-

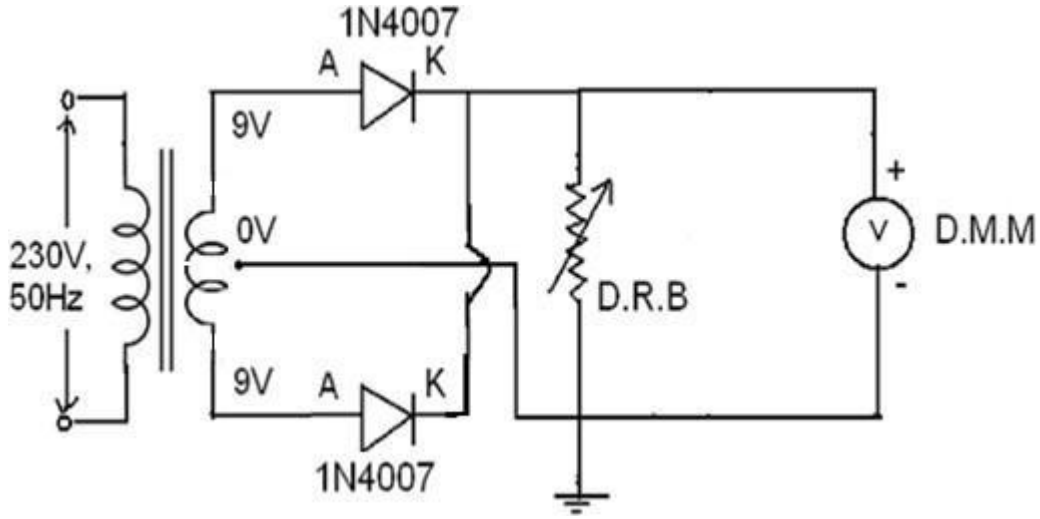
1. Ripple factor of Half wave rectifier was measured

2. The percentage regulation of Half wave rectifier was calculated with filter At RL=

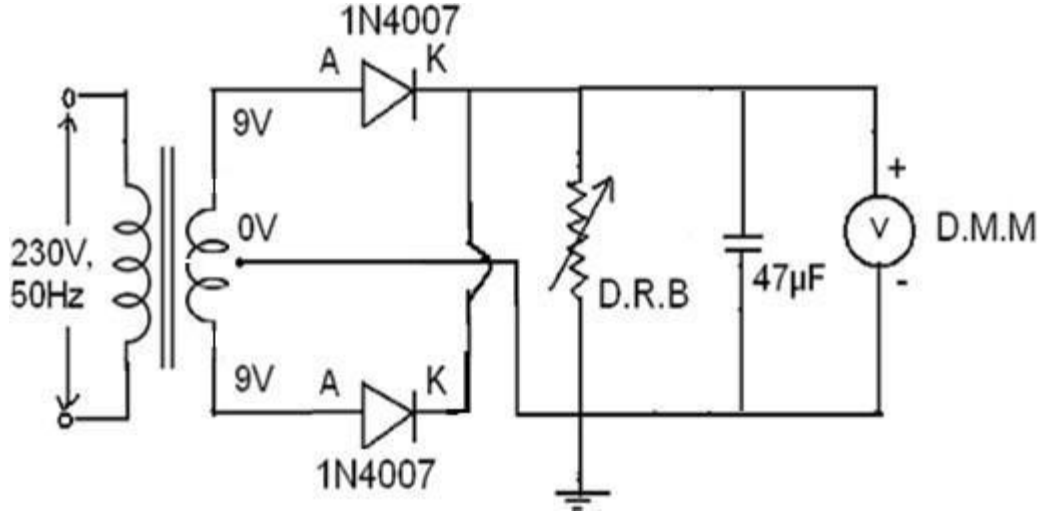
With out Filter	**With Filter**
1. Ripple factor=	1.Ripple factor=
2. % Voltage regulation=	2. % Voltage regulation=

CIRCUIT DIAGRAM:-

WITHOUT FILTER:



WITH FILTER:



EXPERIMENT NO: ***DATE:***

FULL WAVE RECTIFIER WITHOUT AND WITHFILTER

AIM:- To find the Ripple factor and regulation of a Full-wave Rectifier without and with filter.

COMPONENTS & EQUIPMENT REQUIRED *:*

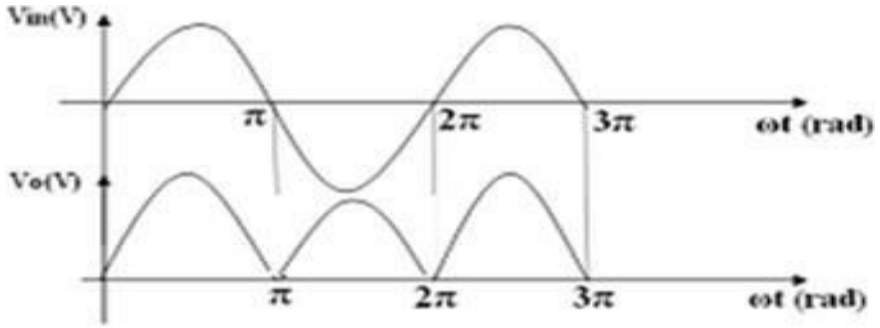
S. NO	NAME OF THE EQUIPMENT	RANGE	QUANTITY
1	Transformer	230V / (9-0-9)v	1
2	PN Junction Diodes	1N 4007	2
3	Multimeter		1
4	Capacitor	47μF	1
5	Connecting Wires	-	Few
6	Decade resistance box	-	1
7	Bread Board	-	1

THEORY:-

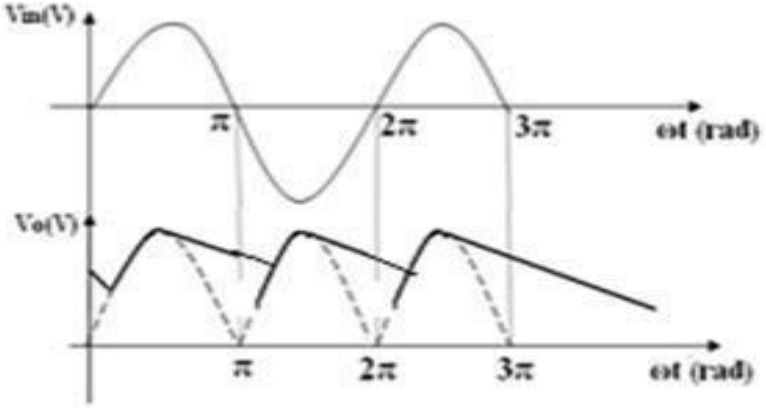
The circuit of a center-tapped full wave rectifier uses two diodes D1&D2. During positive half cycle of secondary voltage (input voltage), the diode D1 is forward biased and D2is reverse biased.
The diode D1 conducts and current flows through load resistor RL. During negative half cycle, diode D2 becomes forward biased and D1 reverse biased. Now, D2 conducts and current flows through the load resistor RL in the same direction. There is a continuous current flow through the load resistor RL, during both the half cycles and will get unidirectional current as show in the model graph. The difference between full wave and half wave rectification is that a full wave rectifier allows unidirectional (one way) current to the load during the entire 360 degrees of the input signal and half-wave rectifier allows this only during one half cycle (180 degree).

MODEL INPUT & OUTPUT WAVE FORMS:-

WITHOUT FILTER :

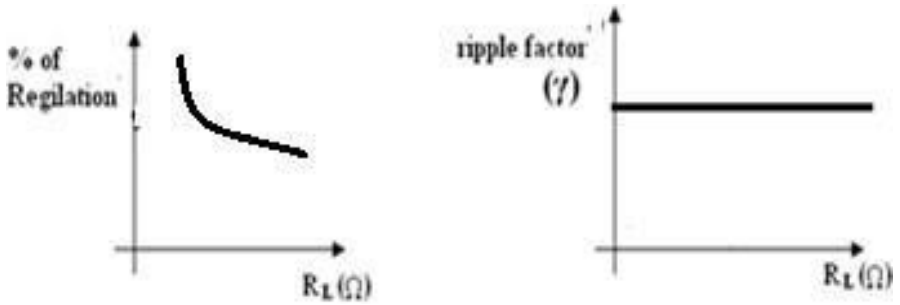


WITH FILTER :

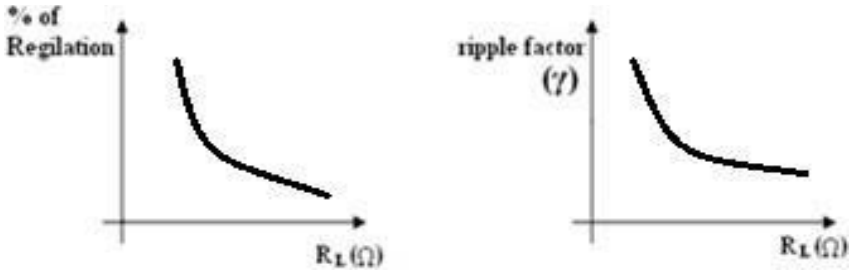


MODEL GRAPHS:

WITHOUT FILTER



WITH FILTER :-



PROCEDURE:

1. Connect the circuit as per the circuit diagram shown in Figure..
2. Note down the No Load DC Voltage Vdc0 when Idc = 0

3. Vary the load resistance RL (DRB) and note down Idc and Vdc, Vac Using Multimeter
   a). Calculate the ripple factor (r)

r = RMS valuesof ACcomponent = Vac
Averagevalue Vdc

b). Calculate the Percentage of Regulation = [(Vd c 0 – Vdc) / Vdc] x 100 (or) (VNL – VFL) / VFL X 100

4. Draw the following graphs

   i). RL Vs Ripple factor

   ii) RL Vs % regulation.

TABULAR COLUMN:-
WITHOUT FILTER :

No Load voltage= 8.44V

S.No.	RL (W)	Idc (mA)	Vdc (V)	Vac (V)	Ripple Factor r = Vac/Vdc	% of Voltage Regulation = [(Vdco – Vdc)/Vdc] X100
1						
2						
3						
4						
5						
6						
7						
8						
9						

TABULAR COLUMN:-
WITHOUT FILTER :

No Load voltage=12.81V

S.No.	RL (W)	Idc (mA)	Vdc (V)	Vac (V)	Ripple Factor r = Vac/Vdc	% of Voltage Regulation = [(Vdco – Vdc)/Vdc] X100
1						
2						
3						
4						
5						
6						
7						
8						
9						

PRECAUTIONS:

1. The primary and secondary sides of the transformer should be carefully identified.
2. The polarities of the diode should be carefully identified.
3. While determining the % regulation, first Full load should be applied and then it should be decremented in steps

Result :

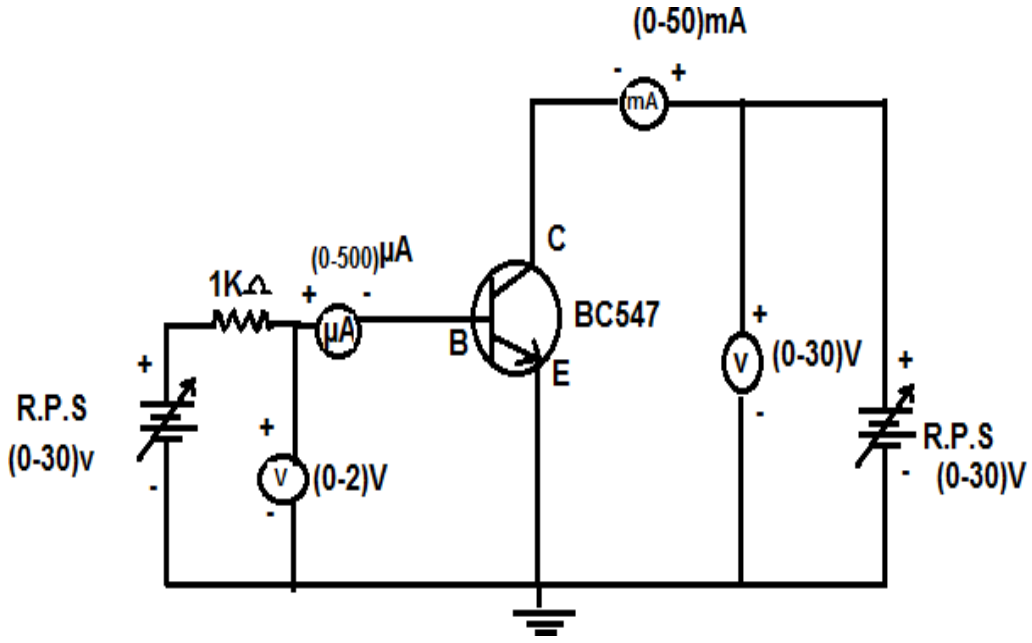
1. **Ripple factor of Fullwave rectifier was measured**

2. **The percentage regulation of Fullwave rectifier was calculated with filter**

At RL= 800 W,

With out Filter	**With Filter**
1. Ripple factor=	**1. Ripple factor=**
2. % Voltage regulation=	**2. % Voltage regulation=**

CIRCUIT DIAGRAM:-



EXPERIMENT NO: ***DATE:***

BJT CE CHARACTERSTICS

AIM: 1. To draw the input and output characteristics of transistor connected in CE configuration

2. To find β of the given transistor.

COMPONENTS & EQUIPMENT REQUIRED *:*

S.NO	NAME OF THE EQUIPMENT	RANGE	QUANTITY
1	Transistor	(BC 547)	1
2	R.P.S	(0-30V)	1
3	Voltmeters	(0-20V)	1
4	Ammeters	(0-500)μA, (0-50)mA	1,1
5	Resistors	1KΩ	1
6	Bread board	-	
7	Connecting Wires	-	Few

THEORY:

A transistor is a three terminal device. The terminals are emitter, base, collector. In common emitter configuration, input voltage is applied between base and emitter terminals and out put is taken across the collector and emitter terminals.

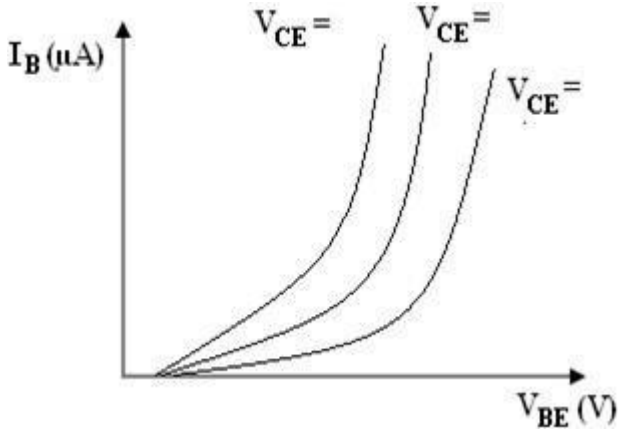
Therefore the emitter terminal is common to both input and output.

The input characteristics resemble that of a forward biased diode curve. This is expected since the Base-Emitter junction of the transistor is forward biased. As compared to CB arrangement I_B increases less rapidly with V_{BE}. Therefore input resistance of CE circuit is higher than that of CB circuit.

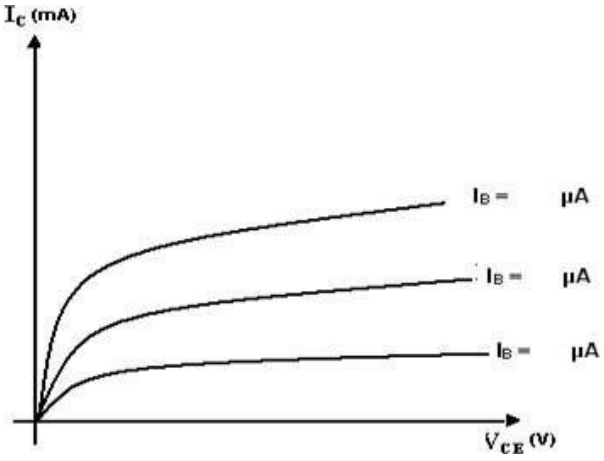
The output characteristics are drawn between I_c and V_{CE} at constant I_B. the collector current varies with V_{CE} unto few volts only. After this the collector current becomes almost constant, and independent of V_{CE}. The value of V_{CE} up to which the collector current changes with V_{CE} is known as Knee voltage. The transistor always operated in the region above Knee voltage, I_C is always constant and is approximately equal to I_B. The current amplification factor of CE configuration is given by $\beta = \Delta I_C / \Delta I_B$

MODEL GRAPHS:

INPUT CHARACTERSTICS:



OUTPUT CHARECTERSTICS:



PROCEDURE:

INPUT CHARECTERSTICS:

1. Connect the circuit as per the circuit diagram.
2. For plotting the input characteristics the output voltage V_{CE} is kept constant at V and for different valuesof V_{BE} . Note down the values of I_C
3. Repeat the above step by keeping V_{CE} at and V.
4. Tabulate all the readings.
5. plot the graph between V_{BE} and I_B for constant V_{CE}

OUTPUT CHARACTERSTICS:

1. Connect the circuit as per the circuit diagram
2. for plotting the output characteristics the input current I_B is kept constant at μA and for different valuesof V_{CE} note down the values of I_C
3. repeat the above step by keeping I_B at μA
4. tabulate the all the readings
5. plot the graph between V_{CE} and I_C for constant I_B

INPUT CHARACTERISTICS:

S.NO	V_{CE} = V		V_{CE} = V		V_{CE} = V	
	V_{BE}(V)	I_B(μA)	V_{BE}(V)	I_B(μA)	V_{BE}(V)	I_B(μA)
1						
2						
3						
4						
5						
6						
7						
8						
9						
10						
11						

OUTPUT CHAREACTARISTICS

S.NO	I_B = μA		I_B = μA		I_B = μA	
	V_{CE}(V)	I_C(mA)	V_{CE}(V)	I_C(mA)	V_{CE}(V)	I_C(mA)
1						
2						
3						
4						
5						
6						
7						
8						
9						
10						
11						

PRECAUTIONS:

1. The supply voltage should not exceed the rating of the transistor
2. Meters should be connected properly according to their polarities

CALCULATIONS:-

Input impedance =

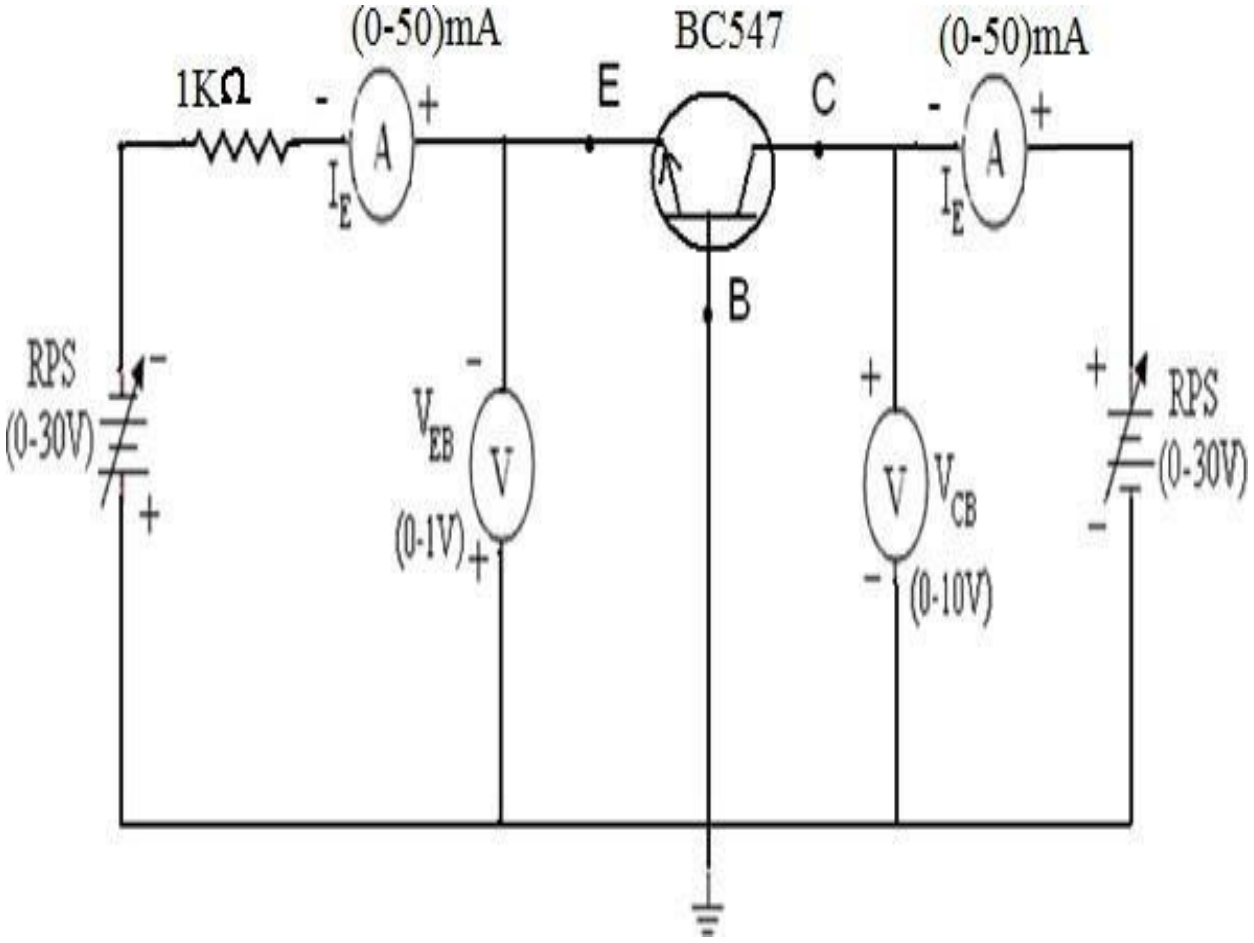
Output impedance =

Current gain =

RESULT:

1. ***The input and output characteristics of the transistor were drawn .***
2. ***The current gain β =***

CIRCUIT DIAGRAM :-



EXPERIMENT NO: ***DATE:***

BJT COMMON -BASE CONFIGURATION

AIM: 1.To observe and draw the input and output characteristics of a transistor connected in common base configuration.

2. To find α of the given transistor.

COMPONENTS & EQUIPMENT REQUIRED *:*

S.NO	NAME OF THE EQUIPMENT	RANGE	QUANTITY
1	Transistor	BC 547	1
2	Regulated power supply	(0-30)V	1
3	Voltmeter	(0-20V),(0-2)V	1,1
4	Ammeters	(0-50)mA,(0-50)mA	1,1
5	Resistor	1KΩ	1
6	Bread board	-	1
7	Connecting wires	-	Few

THEORY:

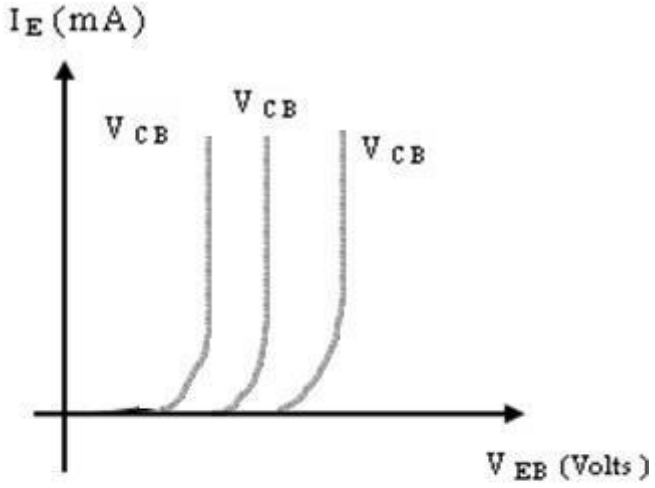
A transistor is a three terminal active device. The terminals are emitter, base, collector. In CB configuration, the base is common to both input (emitter) and output (collector). For normal operation, the E-B junction is forward biased and C-B junction is reverse biased.

With an increasing the reverse collector voltage, the space-charge width at the output junction increases and the effective base width 'W' decreases. This phenomenon is known as "Early effect". Then, there will be less chance for recombination within the base region.

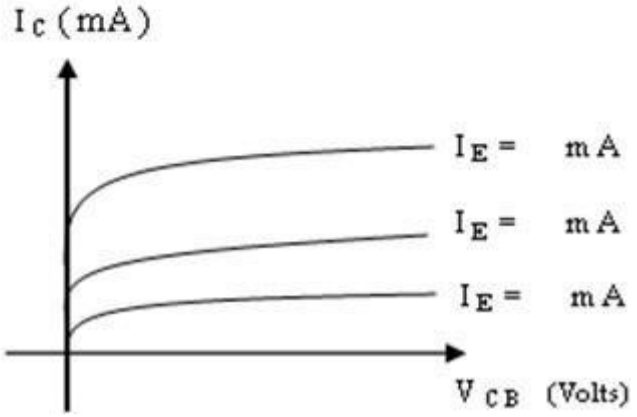
With increase of charge gradient with in the base region, the current of minority carriers injected across the emitter junction increases. The current amplification factor of CB configuration is given by $\alpha = \Delta I_C / \Delta I_E$

MODEL GRAPHS:

Input Characteristics:



Output characteristics:



PROCEDURE:

INPUT CHARACTERISTICS:

1. Connections are made as per the circuit diagram.

2. For plotting the input characteristics, the output voltage V_{CB} is kept constant at 0V and for different values of V_{EB} note down the values of I_E.

3. Repeat the above step keeping V_{CB} at V, V, and V.All the readings are tabulated.

4. A graph is drawn between V_{EB} and I_E for constant $V_{CB.}$

OUTPUT CHARACTERISTICS:

1. Connections are made as per the circuit diagram.
2. For plotting the output characteristics, the input I_E iskept constant at 5m A and for different values of V_{CB}, note
3. down the values of $I_{C.}$
4. Repeat the above step for the values of I_E at mA, mA, and mA, all the readings are tabulated.
5. A graph is drawn between V_{CB} and Ic for constant I_E

TABULAR COLUMN:

INPUT CHARACTERISTICS:

S.No	V_{CB} = V		V_{CB} = V		V_{CB}= V	
	V_{EB}(V)	$I_{E(}$mA)	V_{EB}(V)	$I_{E(}$mA)	V_{EB}(V)	$I_{E(}$mA)
1						
2						
3						
4						
5						
6						
7						
8						
9						
10						

OUTPUT CHARACTERISTICS:

S.No	$I_{E=}$ mA		$I_{E=}$ mA		I_E= mA	
	V_{CB}(V)	$I_{C(}$mA)	V_{CB}(V)	$I_{C(}$mA)	V_{CB}(V)	$I_{C(}$mA)
1						
2						
3						
4						
5						
6						
7						
8						
9						
10						
11						

PRECAUTIONS:

1. The supply voltages should not exceed the rating of the transistor.
2. Meters should be connected properly according to their polarities.

CALCULATIONS:-

Input impedance = $(\Delta V_{EB}V/\ \Delta I_E)\Omega=0.1/3*10^{-3}=33.33\Omega$

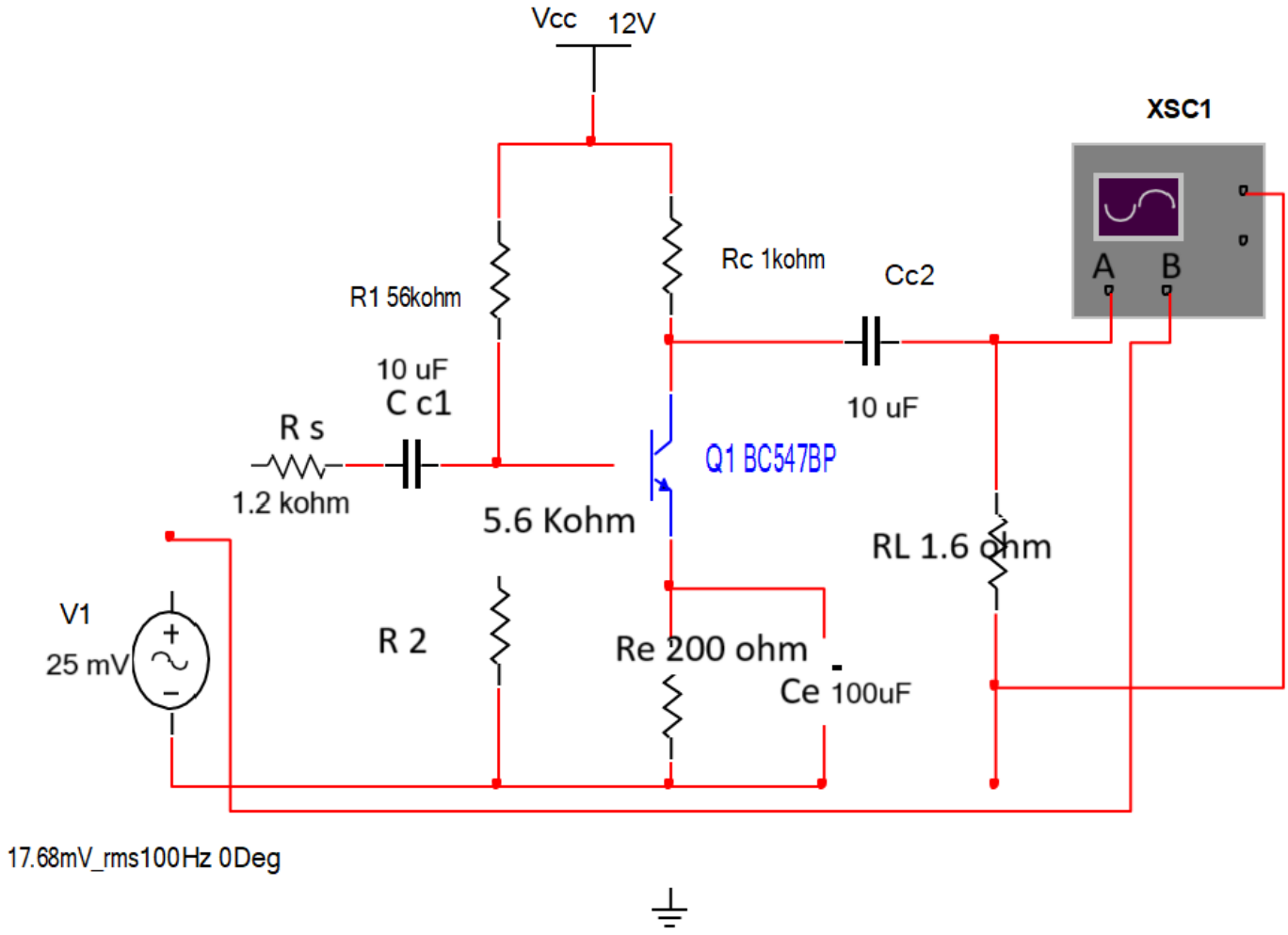
Output impedance $=(\Delta V_{CB}V/\ \Delta I_C)\Omega=0.5/0=\infty$

Current gain $\alpha= \Delta I_C/\ \Delta I_E =5/5=1$

RESULT:

1. ***The input and output characteristics of the transistor were drawn .***
2. ***The current gain α = 1***

CIRCUIT DIAGRAM:-



Expt. No. Date:

FREQUENCY RESPONSE OF CE AMPLIFIER

AIM: - To design and simulate transient response and AC analysis of Single Stage CE Amplifier Circuit to Sinusoidal input by using Multisim PSPICE package and verify the result with Hardware tools.

TOOLS REQUIRED:-

- Software Tools Required:-
  Multisim PSPICE 2001 simulation package.
- Hardware Tools Required:-

COMPONENTS USED:-

S.No.	Name of the Component	Range	Quantity
1.	Transistor	BC 547	1
2.	Resistors	1.2KΩ, 56KΩ, 5.6KΩ, 1KΩ, 200KΩ	1 1 2 1 1
3.	Capacitors	100μf, 10μf	1 2
4.	Regulated power supply	0-30V	1
5.	Dual trace CRO	-	1
6.	Function Generator	10Hz – 10MHz	1

Theory:

Common Emitter Amplifier is widely used in audio frequency applications in radio and TV receivers. It provides current, voltage and power gains. Base current controls the collector current of a common emitter amplifier. A small increase in base current results in a relatively large increase in collector current. Similarly, a small decrease in base current causes large decrease in collector current. The emitter-base Junction must be forward biased and the collector base junction must be reverse biased for the proper functioning of an amplifier.

EXPERIMENTAL PROCEDURE:-

Software:-

(1). Open the Multisim simulation package in the Personal Computer.

(2). Select new file and give the file name.

(3). Build a circuit using component toolbar according to the circuit diagram.

(4). Simulate the circuit using frequency response analysis menu by choosing output variables.

(5). View and store the result.

Hardware: -

1. Connect the circuit as shown in circuit diagram
2. Apply the input of 60mV peak-to-peak and 1 KHz frequency using FunctionGenerator
3. Measure the Output Voltage Vo (p-p) for from 100Hz to 1MHz Using function generator Tabulate the readings in the tabular form.
4. The voltage gain can be calculated by using the expression $A_v = (V_0/V_i)$
5. For plotting the frequency response the input voltage is kept Constant at 60mV peak-to-peak and the frequency is varied from 100Hz to 1MHz using function generator
6. Note down the value of output voltage for each frequency.
7. All the readings are tabulated and voltage gain in dB is calculated by using the expression $A_v = 20 \log_{10} (V_0/V_i)$
8. A graph is drawn by taking frequency on x-axis and gain in dB on y-axison Semi-log graph.

The band width of the amplifier is calculated from the graph

Using the expression, Bandwidth, $BW = f_2 - f_1$

Where f_1 lower cut-off frequency of CE amplifier, and

Where f_2 upper cut-off frequency of CE amplifier

9. Compare the result obtained by Software & Hardware.

TABULAR COLUMN:-

Software:

V_{in} = ----------

Sl. No.	Frequency(Hz)	Output Voltage(V_o)	$A_v = V_o / V_{in}$	Gain (dB) =20*log(A_v)

Hardware:-

V_{in} = ----------

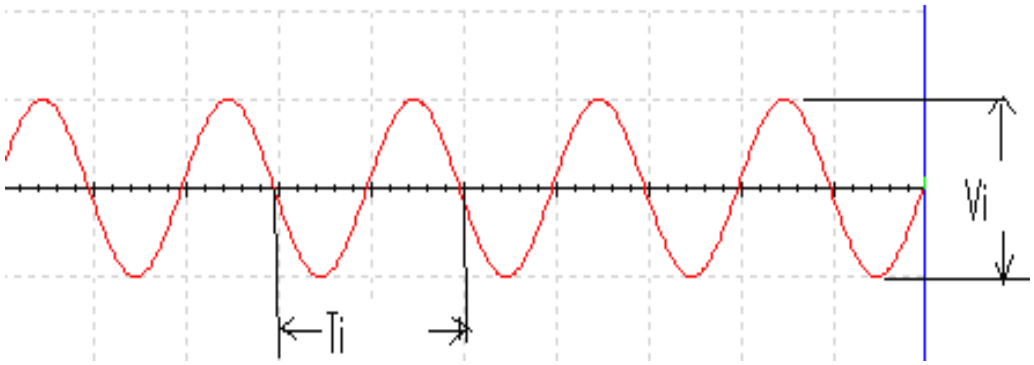
Sl. No.	Frequency (Hz)	Output Voltage(V_o)	$A_v=V_o/V_{in}$	Gain(dB)= 20log(A_v)

Formula:-

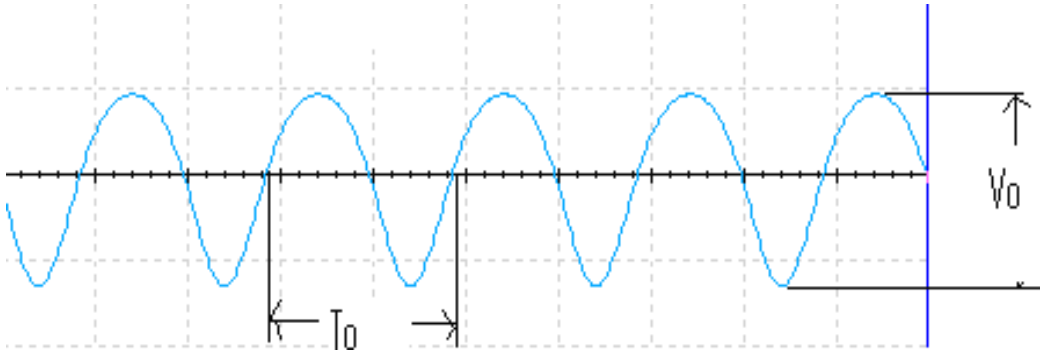
Voltage gain (A_v) = 20* log (V_o / V_i)

MODEL GRAPHS:

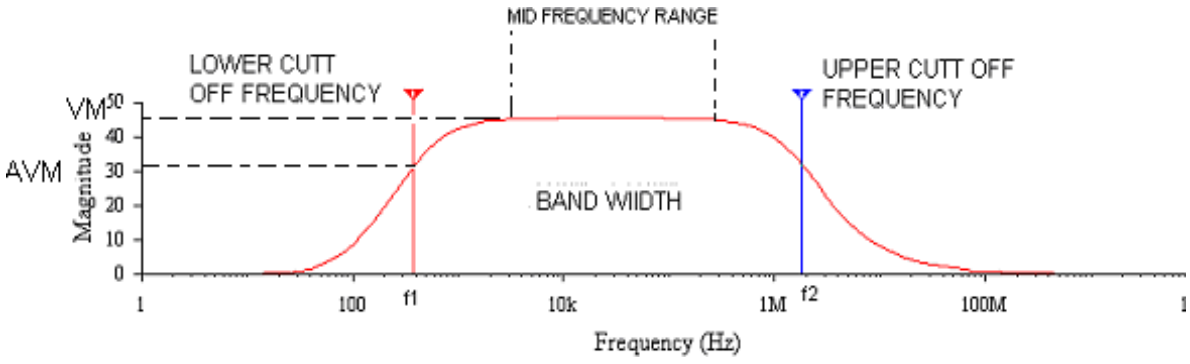
Input Waveform:



Output Waveform:



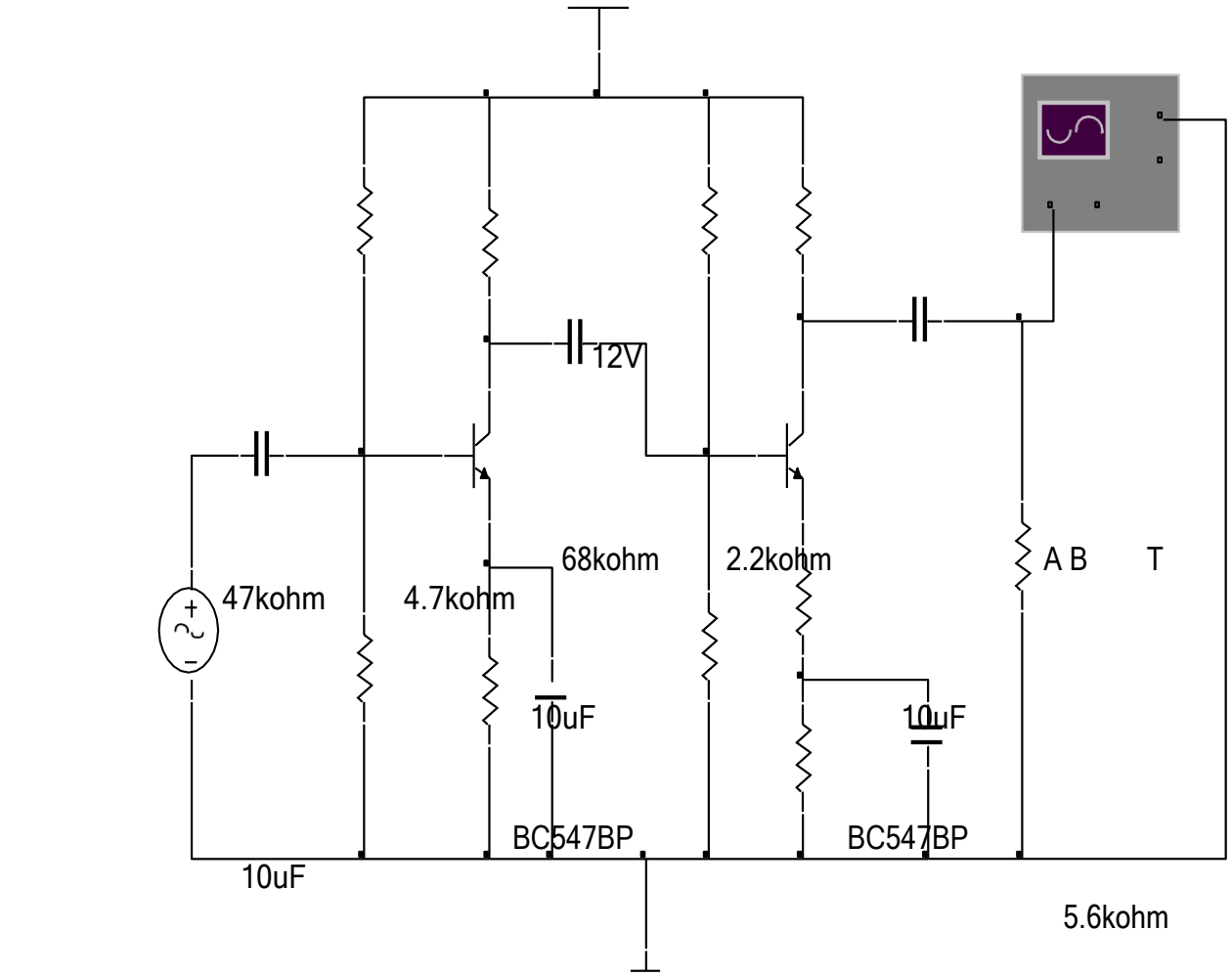
Frequency Response:



COMPARISON TABLE:-

Sl. No	Particulars	Software	Hardware

RESULT:-


12V
68kohm
2.2kohm
A B
T
47kohm
4.7kohm
10uF
10uF
BC547BP
BC547BP
10uF
5.6kohm
10mV 7.07mV_rms100Hz 0Deg
33kohm
220ohm
4.7kohm
220 ohm
100uF
22uF
1.5kohm

Expt. No. Date:

TWO STAGE RC COUPLED AMPLIFIER

AIM: - To design and simulate transient response and AC analysis of Two Stage RC coupled Amplifier Circuit to Sinusoidal input by using Multisim PSPICE package along with Hardware and find the Bandwidth.

TOOLS REQUIRED:-

- Software Tools Required:-
  Multisim PSPICE 2001 simulation package.
- Hardware Tools Required:-

COMPONENTS USED:-

S.No.	Name of the Component	Range	Quantity
1.	Transistor	BC547 BP	2
2.	Resistors	33KΩ, 68 KΩ, 1KΩ, 4.7KΩ, 47KΩ 220Ω 2.2 KΩ 1.5 KΩ 5.6 KΩ	1 1 1 2 1 2 1 1 1
3.	Capacitors	10μf,	3

		100µf 22µf	1 1
4.	Regulated power supply	0-30V	1
5.	Dual trace CRO	-	1
6.	Function Generator	10Hz – 10MHz	1

THEORY:

This is most popular type of coupling as it provides excellent audio fidelity. A coupling capacitor is used to connect output of first stage to input of second stage. Resistances R1, R2,Re form biasing and stabilization network. Emitter bypass capacitor offers low reactance paths to signal coupling Capacitor transmits ac signal, blocks DC. Cascade stages amplify signal and overall gain is increased total gain is less than product of gains of individual stages. Thus for more gain coupling is done and overall gain of two stages equals to A=A1*A2
A1=voltage gain of first stage
A2=voltage gain of second stage.

When ac signal is applied to the base of the transistor, its amplified output appears across the collector resistor Rc.It is given to the second stage for further amplification and signal appears with more strength. Frequency response curve is obtained by plotting a graph between frequency and gain in db .The gain is constant in mid frequency range and gain decreases on both sides of the mid frequency range. The gain decreases in the low frequencyrange due to coupling capacitor Cc and at high frequencies due to junction capacitance Cbe.

EXPERIMENTAL PROCEDURE:-

Software:-

(1). Open the Multisim simulation package in the Personal Computer.

(2). Select new file and give the file name.

(3). Build a circuit using component toolbar according to the circuit

diagram.

(4). Simulate the circuit using frequency response analysis menu by choosing output variables.

(5). View and store the result.

Hardware: -

1. Connect the circuit as shown in circuit diagram
2. Apply the input of 20mV peak-to-peak and 1 KHz frequency using FunctionGenerator
3. Measure the Output Voltage Vo (p-p) for from 100Hz to 1MHz Using function generator Tabulate the readings in the tabular form.
4. The voltage gain can be calculated by using the expression $A_v = (V_0/V_i)$
5. For plotting the frequency response the input voltage is kept Constant at 60mV peak-to-peak and the frequency is varied from 100Hz to 1MHz using function generator
6. Note down the value of output voltage for each frequency.
7. All the readings are tabulated and voltage gain in dB is calculated by using the expression $A_v = 20 \log_{10} (V_0/V_i)$
8. A graph is drawn by taking frequency on x-axis and gain in dB on y-axison Semi-log graph.

The band width of the amplifier is calculated from the graph

Using the expression, Bandwidth, $BW = f_2 - f_1$

TABULAR COLUMN:-

Software:

V_{in} = ----------

Sl. No.	Frequency(Hz)	Output Voltage(V_o)	$A_v = V_o / V_{in}$	Gain (dB) =20*log(A_v)

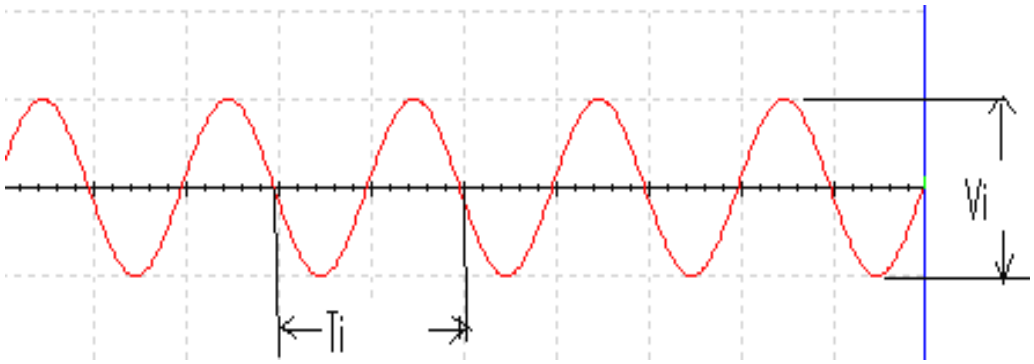
Hardware:

V_{in} = ----------

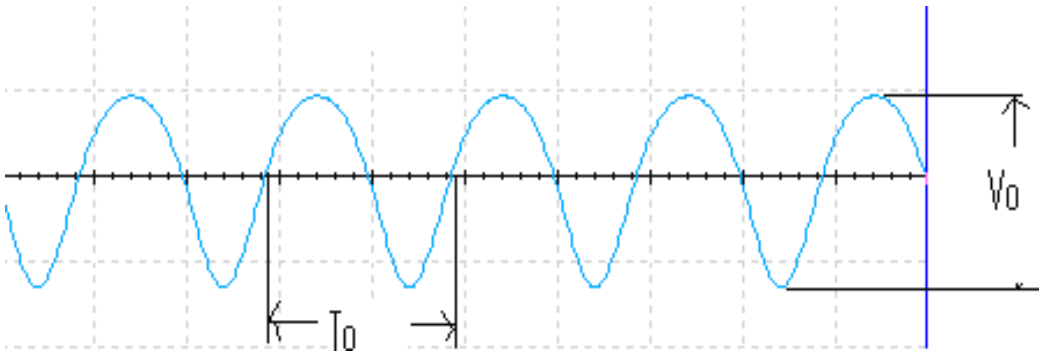
Sl. No.	Frequency(Hz)	Output Voltage(V_o)	$A_v = V_o / V_{in}$	Gain (dB) =20*log(A_v)

MODEL GRAPHS:

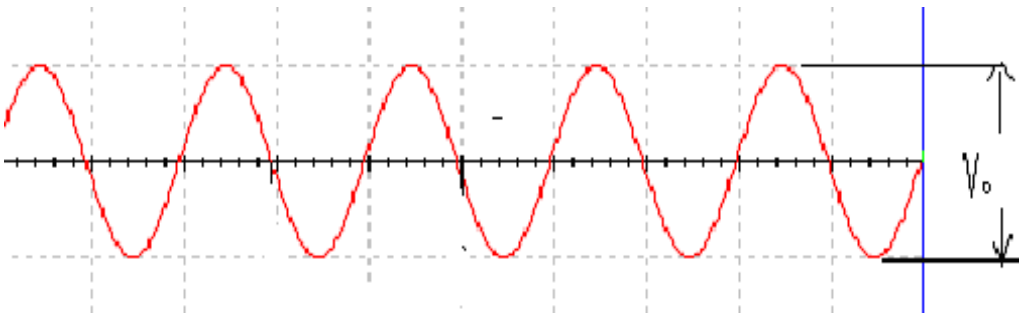
INPUT WAVEFORM:



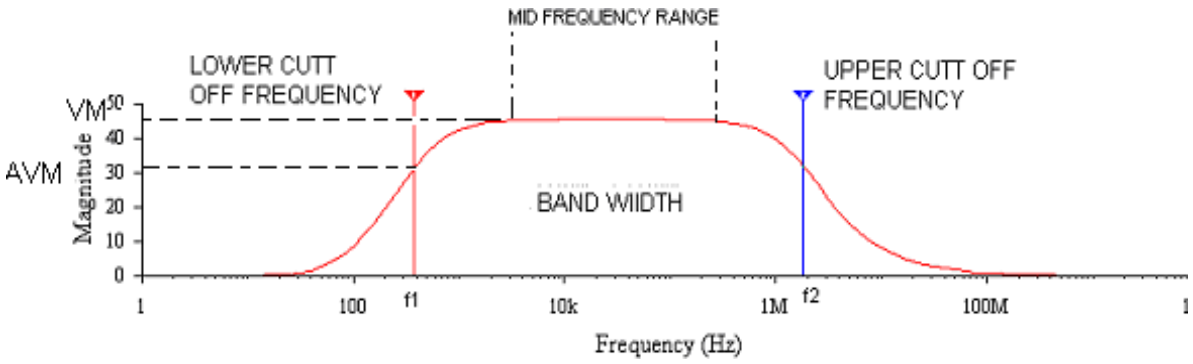
First stage Output Waveform:



Second stage Output Waveform:



FREQUENCY RESPONSE:



Formula:-

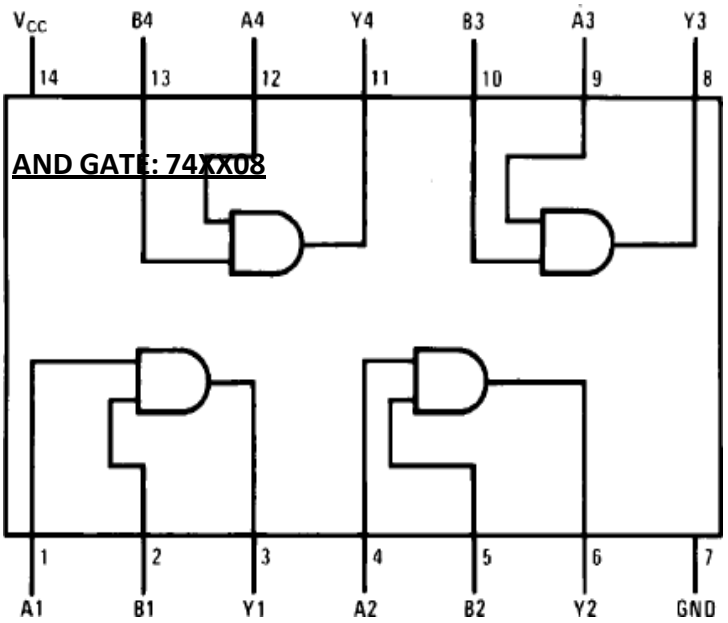
Voltage gain (A_v) = 20 * log (V_o / V_i)

COMPARISON TABLE:-

Sl. No	Particulars	Software	Hardware

RESULT:-

AND GATE: 74XX08



Connection Diagram

$Y = AB$

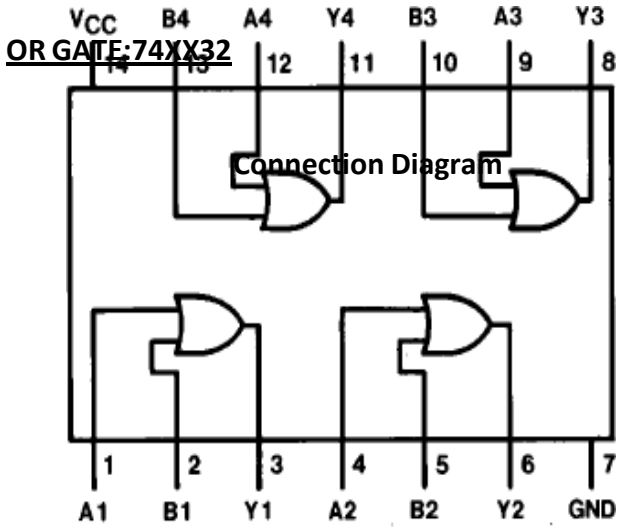
Inputs		Output
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

H = High Logic Level

L = Low Logic Level

Functional Table

OR GATE:74XX32



Connection Diagram

$Y = A + B$

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

H = High Logic Level

L = Low Logic Level

Functional Table

EXPERIMENT NO: ***DATE:***

VERIFICATION OF TRUTH TABLE OF AND, OR, NOT, NAND, NOR, EX-OR, EX-NOR GATES USING ICS.

AIM: To perform an experiment on logic gates by using digital ICs 74XX.

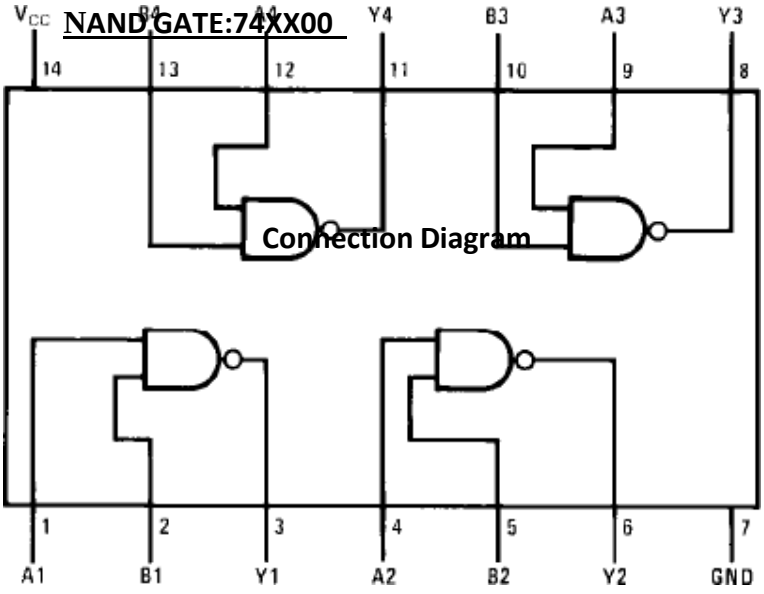
APPARATUS REQUIRED:

S.No	Name of the components	Range	Quantity
1	74LS00-QUAD 2-INPUT NAND GATE 74LS02- QUAD 2-INPUT NOR GATE 74LS04- HEX NOT GATE 74LS08- QUAD 2-INPUT AND GATE 74LS32- QUAD 2-INPUT OR GATE 74LS86- QUAD 2-INPUT EX-OR GATE	-	1
2	Fixed power supply	5V	1
3	LEDS	-	2
4	Connecting Wires	-	10
5	Bread Board	-	1

PROCEDURE FOR HARDWARE VERIFICATION:

1. Check the components for their working.
2. Connect the circuit on breadboard according to the logic symbol.
3. Apply +5V for Vcc & 0V for GND.
4. Provide input data and verify the outputs through LEDs for all input combinationsand compare with truth table.

NAND GATE:74XX00



Connection Diagram

$Y = \overline{AB}$

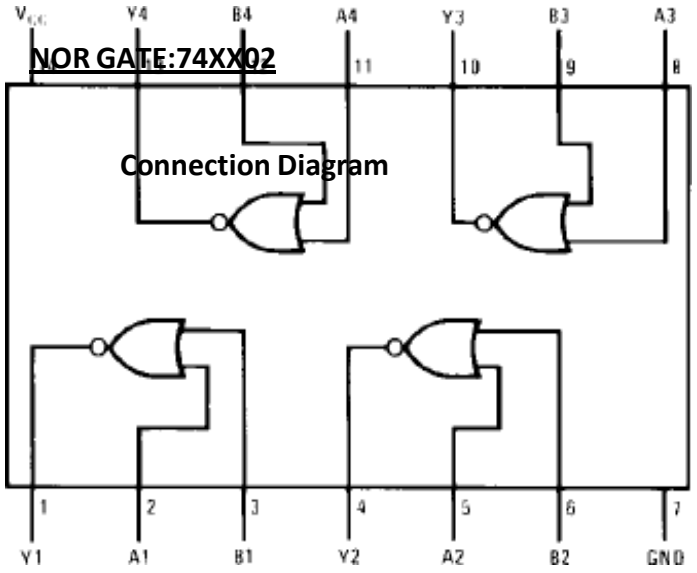
Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

Functional Table

H = High Logic Level

L = Low Logic Level

NOR GATE:74XX02



Connection Diagram

$Y = \overline{A + B}$

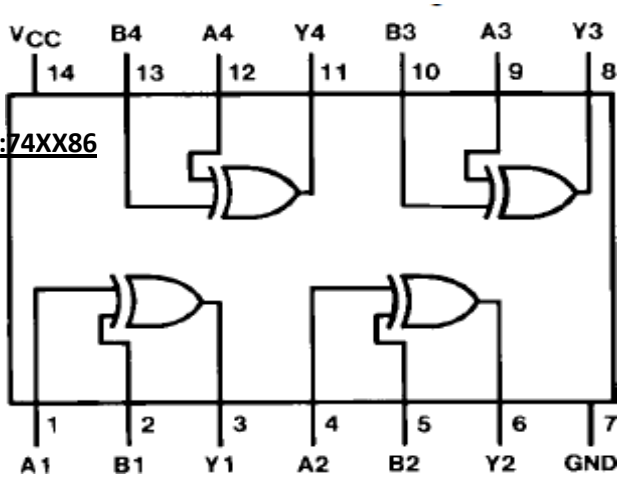
Inputs		Output
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

Functional Table

H = High Logic Level

L = Low Logic Level

EXCLUSIVE-OR GATE:74XX86



Connection Diagram

$$Y = A \oplus B = \overline{A}B + A\overline{B}$$

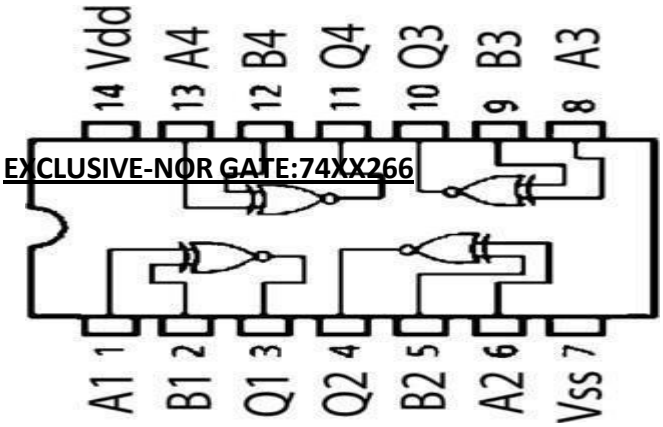
Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = High Logic Level

L = Low Logic Level

Functional Table

EXCLUSIVE-NOR GATE:74XX266



Connection Diagram

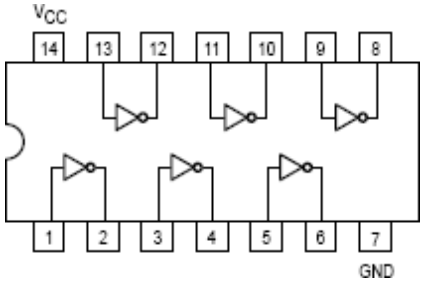
IN		OUT
A	B	Z
L	L	H
L	H	L
H	L	L
H	H	H

Z= A'B'+AB

Functional Table

NOT_GATE:74XX04

Connection Diagram



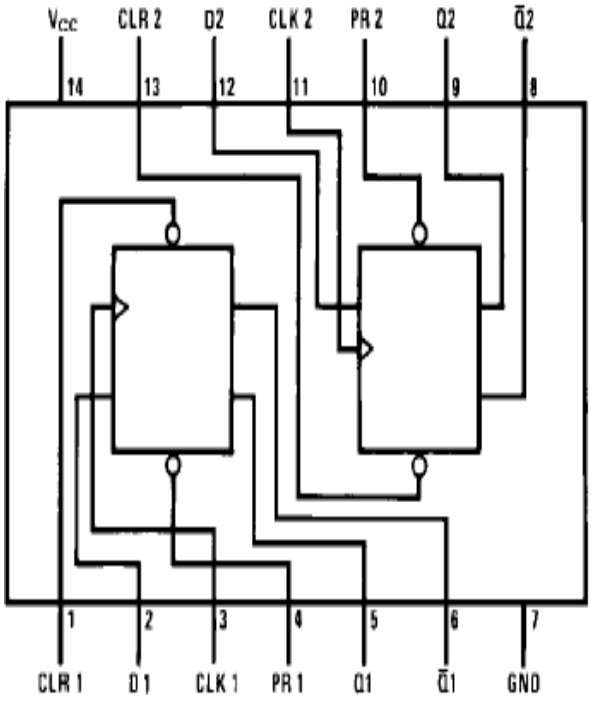
Functional Table: Y=A'

INPUT A	OUTPUT Y
H	L
L	H

RESULT:

D-F LIP FLOP:

Connection diagram



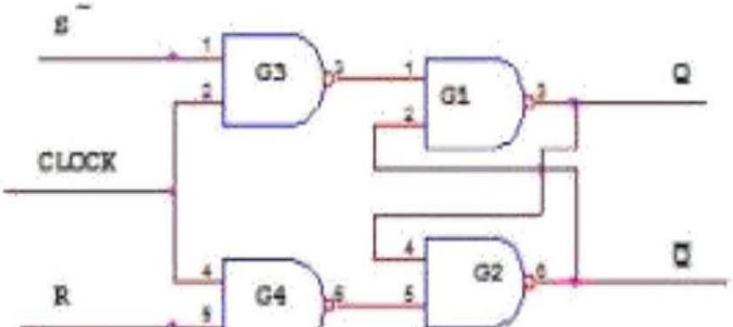
function diagram

Inputs				Outputs	
PR	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H (Note 1)	H (Note 1)
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

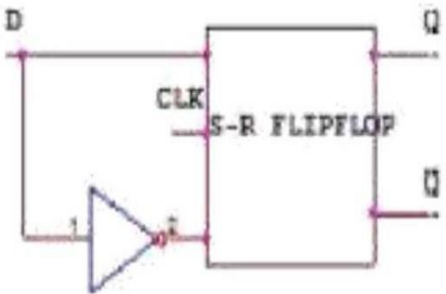
H = HIGH Logic Level
X = Either LOW or HIGH Logic Level
L = LOW Logic Level
↑ = Positive-going Transition
Q_0 = The output logic level of Q before the indicated input conditions were established.

Circuit Diagram :

SR Flip Flop



D Flip Flop



EXPERIMENT NO: ***DATE:***

Verification of Truth Tables of S-R, J-K& D flip flops using respective ICs

AIM:

To perform an experiment on 74LS74 by using hardware circuit & verify its function using truth table

APPARATUS REQUIRED:

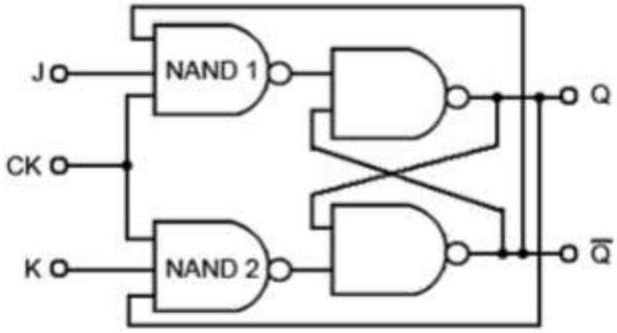
S.No	Name of Apparatus	Range	Quantity
1	74LS74	-	1
2	Fixed power supply	5V	1
3	LEDS	-	2
4	Connecting Wires	-	10
5	Bread Board	-	1

THEORY:

RS FLIP-FLOP: There are two inputs to the flip-flop defined as R and S. When I/Ps R = 0 and S = 0 then O/P remains unchanged. When I/Ps R = 0 and S = 1 the

flip-flop is switches to the stable state where O/P is 1 i.e. SET. The I/P condition is R = 1 and S = 0 the flip-flop is switched to the stable state where O/P is 0 i.e. RESET. The I/P condition is R = 1 and S = 1 the flip-flop is switched to the stable state where O/P is forbidden.

JK Flip Flop



TRUTH TABLE:

SR F LIP FLOP:

CLOCK	S	R	n +1
1	0	0	NO CH ANGE
1	0	1	0
1	1	0	1
1	1	1	?

D FL IPFLOP:

INPUT	OU TPUT
0	0
1	1

JK FLIPFLOP

CLOCK	S	R	Q n +1
1	0	0	NO CH ANGE
1	0	1	0
1	1	0	1
1	1	1	

JK FLIP-FLOP: For purpose of counting, the JK flip-flop is the ideal element to use. The variable J and K are called control I/Ps because they determine what the flip- flop does when a positive edge arrives. When J and K are both 0s, both AND gates are disabled and Q retains its last value.

D FLIP FLOP: This kind of flip flop prevents the value of D from reaching the Q output until clock pulses occur. When the clock is low, both AND gates are disabled D can change value without affecting the value of Q. Onthe other hand, when the clock is high, both AND gates are enabled. In this case, Q is forced to equal the value of D. When the clock again goes low, Q retains or stores the last value of D. a D flip flop is a bistable circuit whose D input is transferred to the output after a clock pulse is received.

PROCEDURE FOR HARDWARE VERIFICATION:

1. Check the components for their working.
2. Connect the circuit on breadboard according to the logic symbol.
3. Apply +5V for Vcc & 0V for GND.
4. Provide input data and verify the outputs through LEDs for all input combinationsand compare with truth table.

RESULT: